3.5.1 CLOCK DIVIDER

The RTCC timer must be provided with a 1/2 second (2 Hz) clock source. This is done by selecting appropriate values for the clock prescaler and the variable clock divider.

The clock prescaler divides the input clock by one of four fixed ratios. It is controlled by the PS<1:0> bits (RTCCON2L<5:4>). Divider options are 1:1, 1:16, 1:64 and 1:256.

The variable coarse clock divider further divides the clock input from the prescaler. It provides the entire range of integer divisor options, from 1:1 to 1:32,768. It is controlled by the DIV<15:0> bits field (RTCCON2H<15:0>).

The clock divider also has a fine divider, controlled by the FDIV<4:0> bits. This permits fine frequency adjustments to the timer output. This