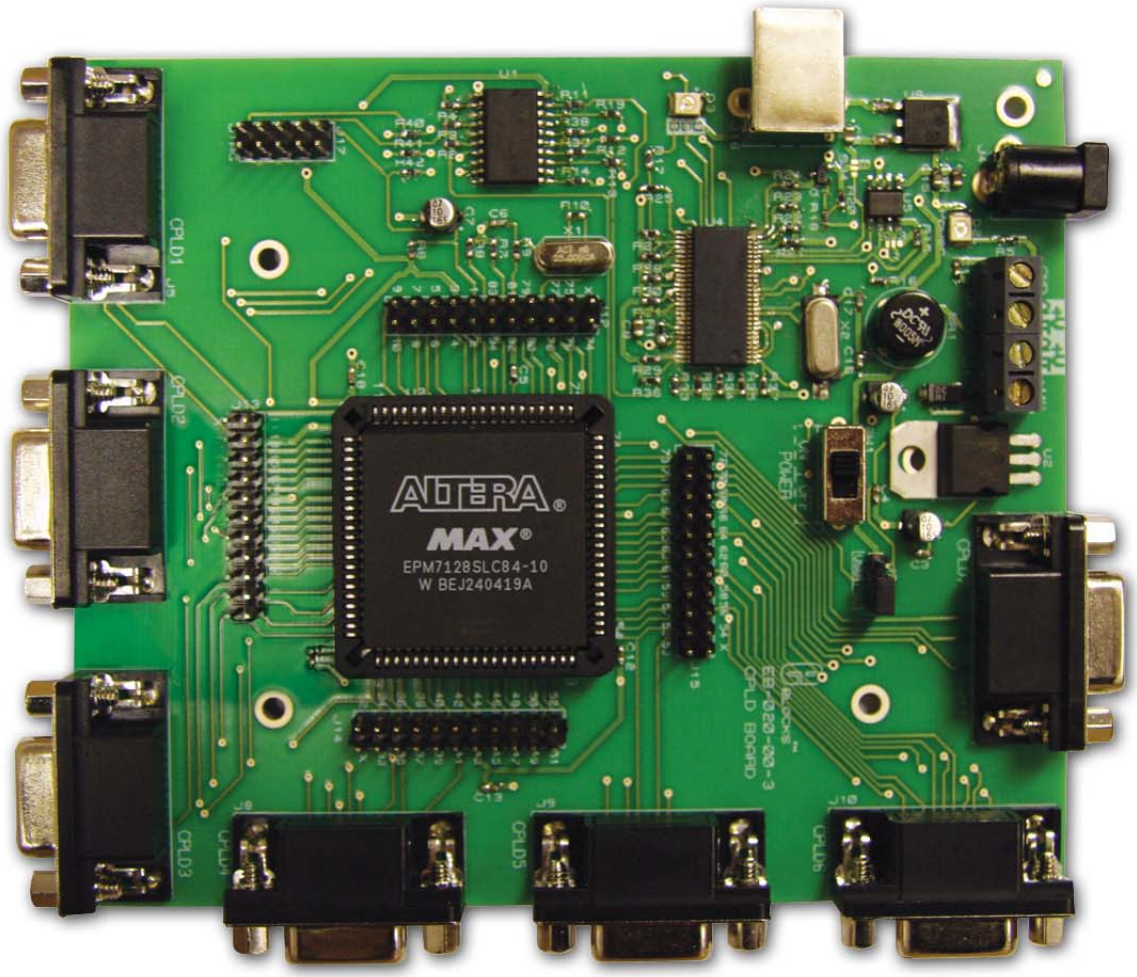
# CPLD board datasheet
# EB020-00-3




## Contents



# 1. About this document

This document concerns the E-blocks CPLD board, code EB020 version 3.

The order code for this product is EB020.

## 1. Trademarks and copyright



## 2. Other sources of information

There are various other documents and sources that you may find useful:

### Getting started with E-Blocks.pdf

This describes the E-blocks system and how it can be used to develop complete systems for learning electronics and for PICmicro programming.

### PPP Help file

This describes the PPP software and its functionality. PPP software is used for transferring hex code to a PICmicro microcontroller.

### C and assembly strategies

This is available as a free download from our web site.

## 3. Disclaimer

The information in this document is correct at the time of going to press. Matrix Multimedia reserves the right to change specifications from time to time. This product is for development purposes only and should not be used for any life-critical application.

## 4. Technical support

If you have any problems operating this product then please refer to the troubleshooting section of this document first. You will find the latest software updates, FAQs and other information on our web site: www.matrixmultimedia.com . If you still have problems please email us at: support@matrixmultimedia.co.uk.

# 2. General information

## 1. Description

This CPLD Board connects to your PC via a standard USB cable to provide you with a low cost CPLD development board and programmer. The board is fully compatible with a wide range of E-blocks which makes it an extremely flexible platform for learning and developing projects.

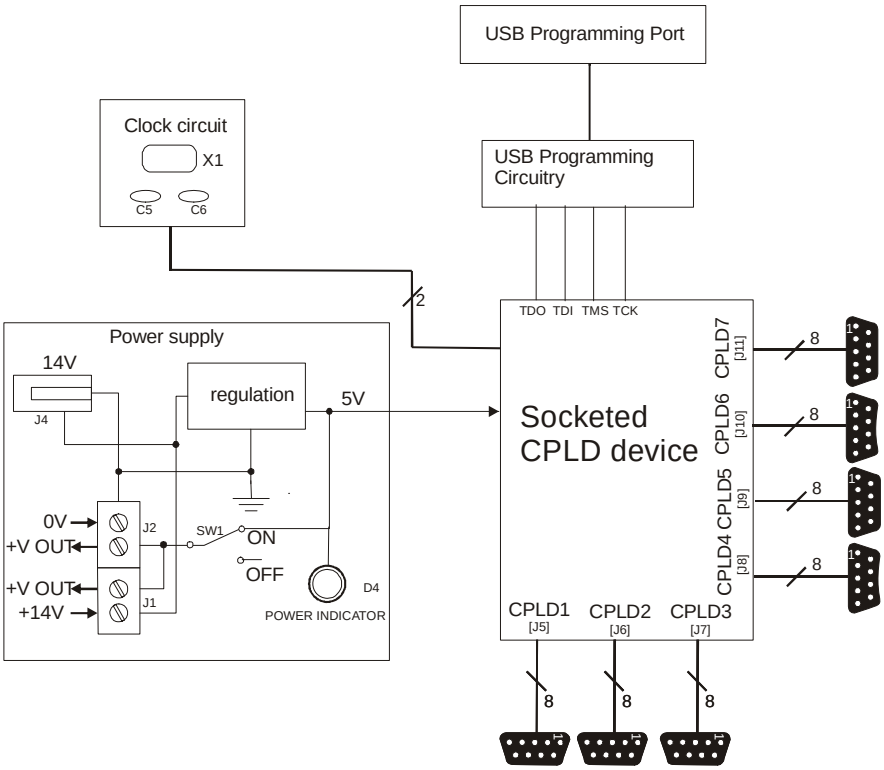
The CPLD Board allows in-circuit programming of an ALTERA® CPLD device. This board is used together with Altera's free and comprehensive downloadable CPLD program, Quartus II. The board can be programmed using various programming techniques such as Schematic Entry, Block Diagram and Hardware Description Languages (HDLs such as AHDL, VHDL and Verilog). It provides 'clean' access to all available I/O lines on the relevant CPLD device.

Further information on E-blocks is available in a separate document entitled Introduction to E-blocks.doc.

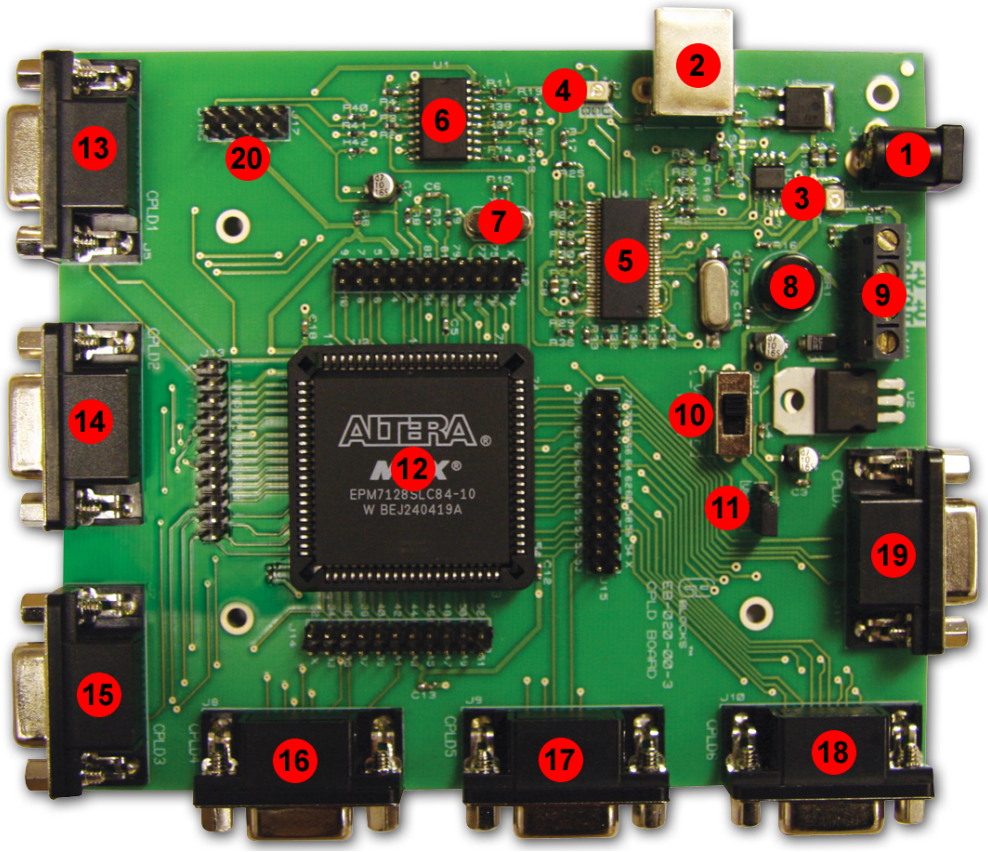
## 2. Features

- E-blocks compatible
- Used as a programmer and as a development board
- Full suite of programming software
- 25MHz Xtal operation
- 7 full I/O ports

## 3. Block schematic



# 3. Board layout




EB020-74-3.cdr

1) Power connector
2) USB connector
3) Power LED Indicator
4) USB LED Indicator
5) USB Host Device
6) Programming Buffer
7) CPLD Crystal
8) Bridge Rectifier
9) Power Screw Terminals
10) Power Switch
11) Power Mode Switch (PSU / USB)
12) ALTERA CPLD and Socket
13) Port - CPLD1
14) Port – CPLD2
15) Port – CPLD3
16) Port – CPLD4
17) Port – CPLD5
18) Port – CPLD6
19) Port – CPLD7
20) ALTERA JTAG Header

# 4. Testing this product

## 1. Installing Quartus II

This software a web-based and therefore requires the users to have access to the Internet.

1) Enter the Altera® website at www.altera.com
2) Click 'Design software' under the product header.
3) Now click 'Downloading" under the Ordering & Downloading header.
4) Next, click "Quartus II Web Edition".
5) Follow the on-screen instructions to download the program
6) Please note that this will involve registering to the Altera website.
7) On completion of the on-screen instructions Quartus II web edition will be fully installed and ready to use.
8) For the most up-to-date version of this software please visit the Altera web page at: www.altera.com

## 2. Test Procedure

The following instructions explain the steps to test and use your CPLD Board. The instructions assume that Quartus II Web Edition is installed and functional. It assumes that the folder "Flasher" has been copied to a suitable place on your computer.

Follow these instructions to test the CPLD Board

1) Ensure power is supplied to the CPLD Board necessary boards.
2) Insert EB-004 LED board into any Port of the CPLD Board
3) Ensure that the power switch (SW1) is in the "ON" position
4) Open Quartus II
5) Open the flasher project
6) Navigate to the flasher folder using the pop-up window
7) Double click on "flasher.quartus"
8) From the Tools menu open up the programmer
9) Tools -> Programmer
10) Click on the following boxes to highlight the programming options
11) Program / Configure
12) Verify
13) Click on "Start Programming" Icon 
14) This should send the program to the CPLD
15) If there is a problem check all cables are connected
    1. Check that all the LEDs on the LED board light up
16) The sequence is as follows
    1. Each light should light consecutively
    2. Then all should stay on
17) You can reset the program by removing the power supply., or switching SW1 to the "OFF" position then to "ON" can perform reset

This should satisfy that the CPLD Board is fully functional!

# 5. Circuit description

The CPLD Board solution is made up of two parts: A circuit board that allows slave CPLD devices to be programmed, and the program to be executed 'seamlessly', and the Windows based programming utility Quartus II Web Edition.

## 1. Power Supply

The board can be powered from a 14V supply. The regulation circuitry will withstand unregulated 20V as a maximum input voltage and 7V as a minimum. If you are using a DC power supply then you should use a 14V setting. Power can be connected using the 2.1mm power jack (positive outer), or the screw terminal connectors J1, J2. The two "+V OUT" screw terminals are supplied for powering other E-blocks™, supplying approximately +5V. The regulator will supply up to 400mA via all outputs. LED D4 will indicate that power is connected to the board and that the voltage regulation circuitry is fully functional.
*Please note* connector J4 is directly connected to the J1 screw terminal pin 1 labeled '+14V', therefore any voltage input to J4 will also be available direct from pin 1 of J1.

### Note

Remember that other E-blocks will have to receive +5V by placing a connecting wire from the "+V Out" screw terminal of the Multiprogrammer to the "+V" screw terminal of each E-Block that requires a voltage.

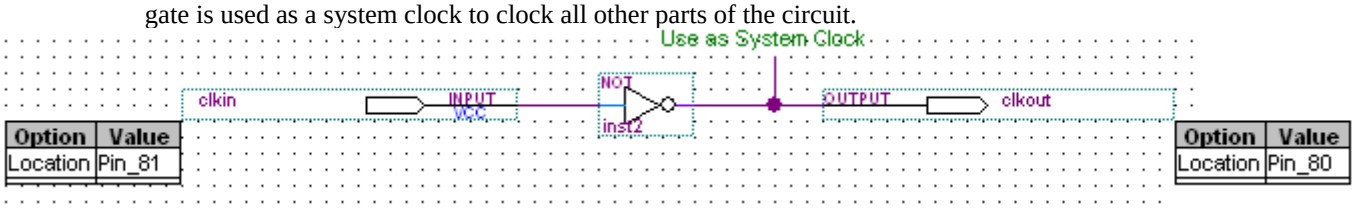
## 2. The CPLD

The CPLD that comes with this board is an 84-pin PLCC Altera® MAX® 7000 series device. The device has 2500 usable gates with 128 Macrocells available. The device has a maximum of 68 I/O lines (note some of them are multiplexed for dual use). This CPLD board utilizes 56 I/O pins, thus providing plenty of resources to set up both simple and complex projects.

## 3. Crystal operation

The board is fitted with a 25MHz crystal. To make use of the 25MHz crystal, your design must include a "not gate" function between the crystal input (Pin 81) and the crystal output (Pin 80). The system clock can be taken from the output of the not gate.

The following diagram shows the block schematic, using Quartus, for the necessary circuit to enable the 25MHz crystal. The "clk_in" input is connected to Pin location 81; this is the physical pin for the crystal input. The "clk_out" input is connected to Pin location 80; this is the physical pin for the crystal output. The output of the not gate is used as a system clock to clock all other parts of the circuit.




Drawing showing the clock schematic block to enable 25MHz

The following is an example Verilog code to enable the crystal in the design. This design uses the same name as the clock schematic above.

```
/********* Crystal oscillator ***********/
always @ (clk_in)
      begin
            clk_out = !clk_in
      end
/*************************************/
```

An example of VHDL code to use the crystal in your design is shown below. Again this code uses the same names as the above clock schematic.

```
-------------------------------------------------------------------
entity clock_gen is port(
      clk_in: in std_logic;
      clk_out: out std_logic);
end clock_gen;

architecture behave of clock_gen is
begin
      process (clk_in)
            begin
                  clk_out <= not clk_in;
      end process;
end behave;
-------------------------------------------------------------------
```

## 4. DIL Headers and I / O Ports

The CPLD DIL Headers (J12, J13, J14 and J14) are wired to the exact replica of the CPLD pins. The numbers surrounding these 4 DIL header pins shows pin of the CPLD device each header pin is connected to. Please note that the 4 header blocks have 22 pins each and therefore one is not connected, which is marked with an "X" on the board.

There are 56 dedicated I/O lines fed out to 7 D-type sockets grouped in ports, each port having 8 I/O lines. The pin-out of these ports can be found below

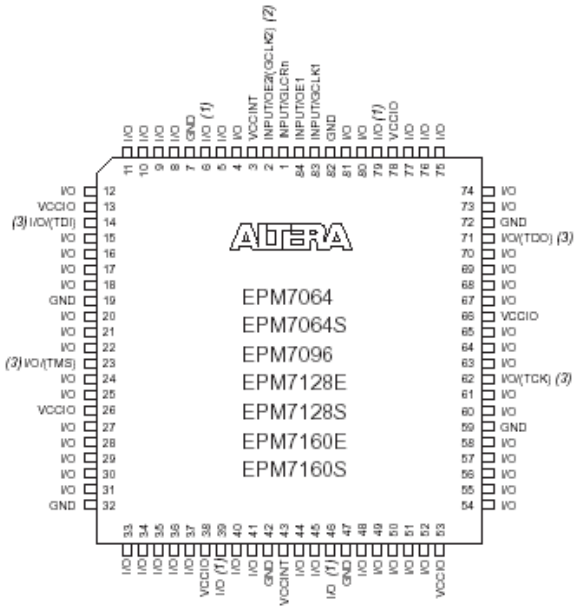
*NOTE* All I/O available are clean signals – this means there is no protection. The user must be aware of this when selecting the functionality of the pins. Avoid connecting +V directly to an I/O pin or two outputs pins directly together – this *can* damage the CPLD device.

## 5. USB circuitry

The EB020 CPLD FPGA Board makes use us a USB socket to provide the programming functionality. Note that the Altera Quartus II software thinks that it is talking to a parallel port or LPT port when it is talking to the Byteblaster cable. This is normal as the USB driver chip is actually emulating a parallel port.

## 6. Device pin out

The following diagram shows the pin-out of the Alter® MAX® EPM128SLC84 device that comes with this board.




84-Pin PLCC

## 7. Port connections

The following table shows the pin connections on the 9-way D-type ports. This should be used for correctly setting the Pin location in the Quartus software.

| **CPLD1** D-type pin number | EPM7128 pin number |
|---|---|
| 1 | IO 4 |
| 2 | IO 5 |
| 3 | IO 6 |
| 4 | IO 8 |
| 5 | IO 9 |
| 6 | IO 10 |
| 7 | IO 11 |
| 8 | IO 12 |
| 9 | GND |

| **CPLD5** D-type pin number | EPM7128 pin number |
|---|---|
| 1 | IO 46 |
| 2 | IO 48 |
| 3 | IO 49 |
| 4 | IO 50 |
| 5 | IO 51 |
| 6 | IO 52 |
| 7 | IO 54 |
| 8 | IO 55 |
| 9 | GND |

| **CPLD2** D-type pin number | EPM7128 pin number |
|---|---|
| 1 | IO 15 |
| 2 | IO 16 |
| 3 | IO 17 |
| 4 | IO 18 |
| 5 | IO 20 |
| 6 | IO 21 |
| 7 | IO 22 |
| 8 | IO 24 |
| 9 | GND |

| **CPLD6** D-type pin number | EPM7128 pin number |
|---|---|
| 1 | IO 56 |
| 2 | IO 57 |
| 3 | IO 58 |
| 4 | IO 60 |
| 5 | IO 61 |
| 6 | IO 63 |
| 7 | IO 64 |
| 8 | IO 65 |
| 9 | GND |

| **CPLD3** D-type pin number | EPM7128 pin number |
|---|---|
| 1 | IO 25 |
| 2 | IO 27 |
| 3 | IO 28 |
| 4 | IO 29 |
| 5 | IO 30 |
| 6 | IO 31 |
| 7 | IO 33 |
| 8 | IO 34 |
| 9 | GND |

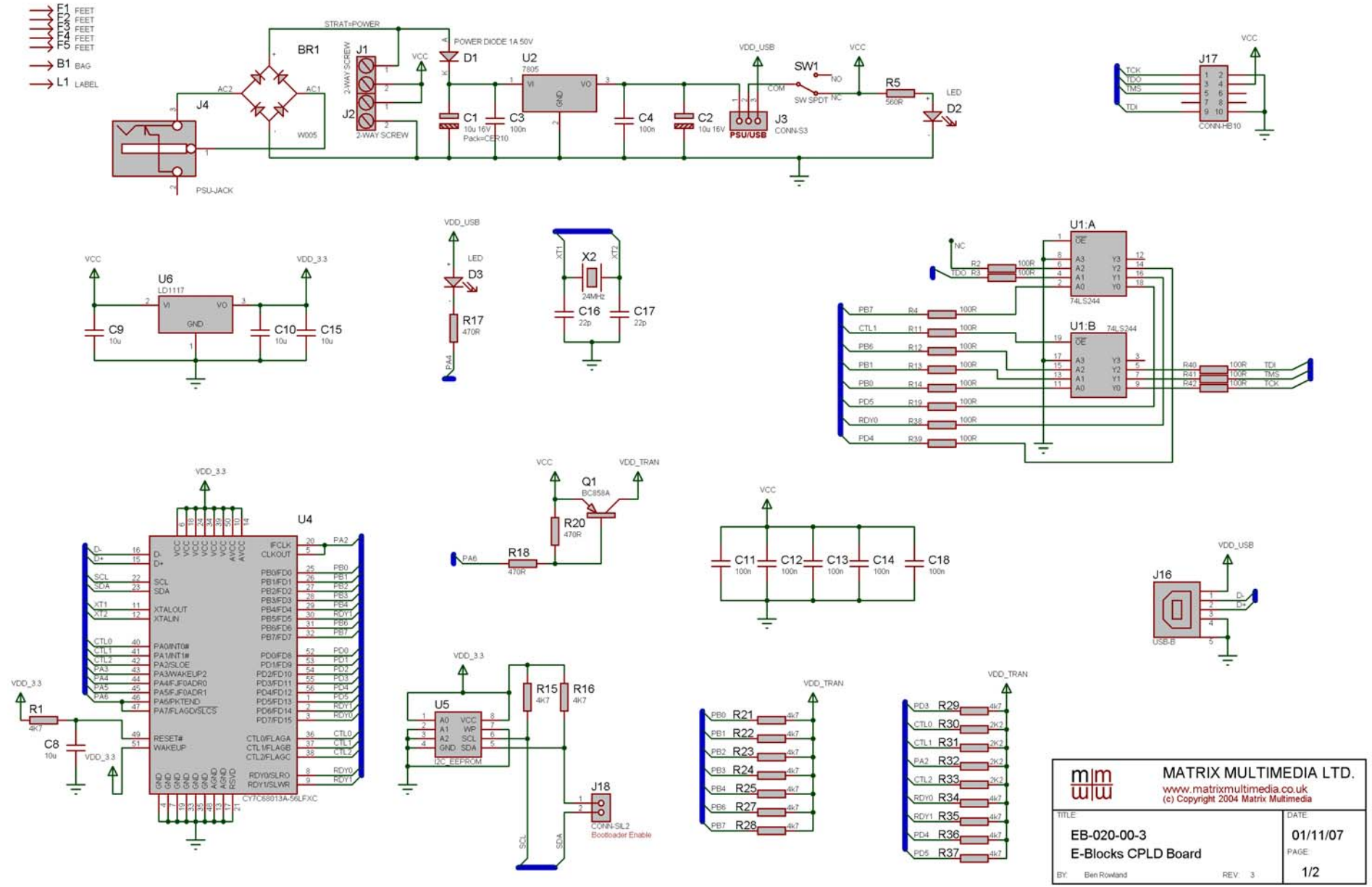
| **CPLD7** D-type pin number | EPM7128 pin number |
|---|---|
| 1 | IO 67 |
| 2 | IO 68 |
| 3 | IO 69 |
| 4 | IO 70 |
| 5 | IO 73 |
| 6 | IO 74 |
| 7 | IO 75 |
| 8 | IO 76 |
| 9 | GND |

| **CPLD4** D-type pin number | EPM7128 pin number |
|---|---|
| 1 | IO 35 |
| 2 | IO 36 |
| 3 | IO 37 |
| 4 | IO 39 |
| 5 | IO 40 |
| 6 | IO 41 |
| 7 | IO 44 |
| 8 | IO 45 |
| 9 | GND |

## 8. 3.3V operation

This board is not compatible with 3.3V systems.

THIS SYSTEM INCLUDES:-

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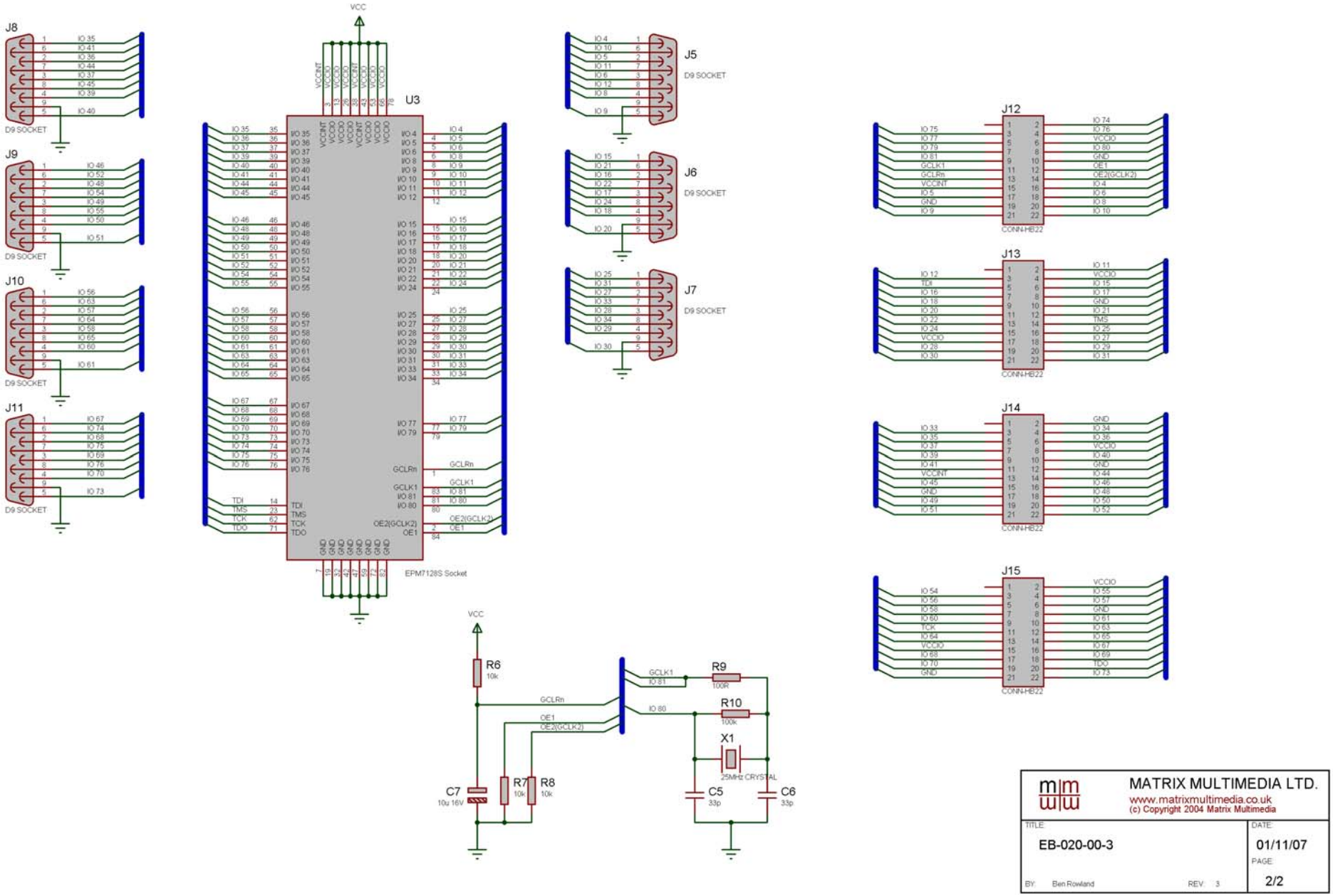
| BY: Ben Rowland REV: 3 | PAGE: 1/2 |

Appendix 1 – Circuit diagram

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