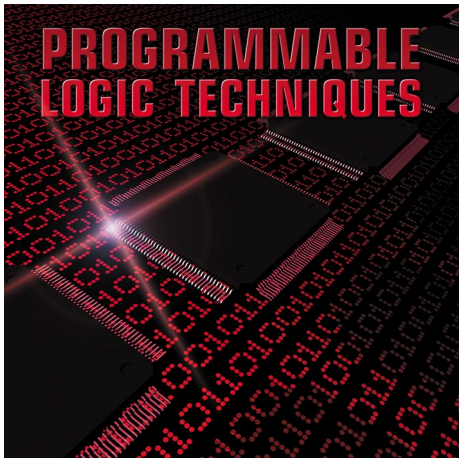
Programmable logic techniques CD ROM

What does it do?

A CD ROM for learning CPLD and FPGA programming using VHDL or Verilog.



Benefits

- A complete course and programming utilities on one CD
- Helps you become a competent programmable logic designer

Features

- Complete guide to logic design using Quartus II
- Includes example projects and exercises
- Includes courses in both Verilog and VHDL
- A modern way to learn digital electronics design
- Compatible with E-blocks CPLD and FPGA development boards

Description

This CD ROM gives a thorough introduction to programmable logic design techniques for CPLDs and FPGAs using Altera's Quartus II Web Edition software. The CD starts with an introduction to designing with Quartus II using block diagrams, at basic and intermediate levels. Then the CD ROM takes students through the process of developing combinational and sequential logic designs using both Verilog and VHDL descriptor languages. The CD is suitable for those who have some experience of digital logic and want to get to grips with modern CPLD and FPGA techniques. A number of example projects in block diagrams, Verilog and VHDL are included, and the CD contains exercises which are suitable as a basis for assessment.

Learning time

Approximately 20 hours in either VHDL or Verilog

Prerequisites

- An reasonable understanding of digital electronics—both combinational and sequential logic
- Windows skills

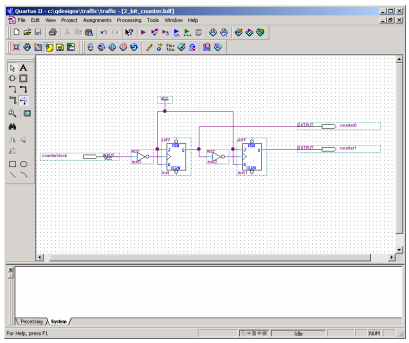
Included on the CD ROM

- Complete course in CPLD programming using Verilog
- Complete course in CPLD programming using VHDL
- Free Quartus II Web edition design software—requires registration

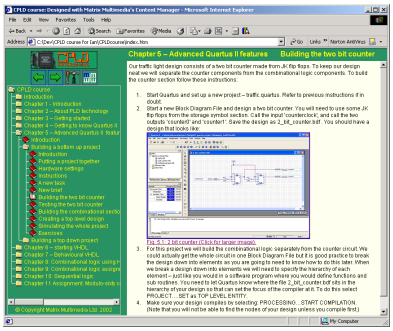
How to use this CD ROM

This CD ROM can be used as a programme of self study at home or in industry. It is also suitable for use with undergraduates as part of a structured course, thereby freeing up lecturers to provide one-to-one tutorial assistance.

Screen images



Quartus II design software



Typical tutorial screen

Also consider

EB020 CPLD programming board
EB030 FPGA board
EB287 CPLD solution
EB940 FPGA solution

CPLD board

CPLD solution

Programmable logic techniques CD ROM

Learning objectives

Study of the CD ROM—will achieve the following objectives:

- Students will become proficient in the Quartus II development system
- Students will understand how to design combinational logic systems for programmable logic devices using VHDL or Verilog
- Students will understand how to design sequential logic systems for programmable logic devices using VHDL or Verilog
- Students will gain the skills required to build complete programmable logic systems
- Students will be able to use theses skills for further project work and assignments.

CD ROM contents

Chapter 1- about this course

Chapter 2- about PLD technology

The basics of PLD and PLA architecture, why use a PLD, Differences between a PLD and a FPGA.

Chapter 3- Getting started

Setting up hardware, pin connections.

Chapter 4 - Getting to know Quartus II

Hierarchy and design flow, Quartus GUI, Elements of Quartus, Subroutines, Entering a simple design from scratch, Design flow.

Chapter 5 - Advanced Quartus features

Building a project bottom up, Building a project top down.

Chapter 6 - An introduction to scripting languages

Verilog design entry, VHDL design entry, Exercises.

Chapter 7- Behavioural descriptions

Introduction, Using a simulator, Verilog two way multiplexer, VHDL two way multiplexer, Indentation of code, Difficulties of Quartus, Quartus simulation, Exercise 1, Exercise 2.

Chapter 8 - Combinational logic using HDL

Design of a 3-input voting machine, Decoders, Encoders, Comparators, Parity checker exercise, Gray to binary converter, Adders, Subtractors and multipliers. All sections are covered in both VHDL and Verilog.

Chapter 9 - Combinational logic assignments

Task 1, Task, 2, Task 3, Task 4, Task 5.

Chapter 10 - Sequential logic

Introduction, The S-R latch, The D-type flip flop, The JK-type flip flop, Asynchronous up counter, Asynchronous BCD up counter, Synchronous counters, Synchronous binary counters, Synchronous binary up counter, Synchronous 0-5 up-down counter, Behavioural description of counters, Another state machine. All sections are covered in both VHDL and Verilog.

Chapter 11: modulo sixty counter assignment

Versions available

ELPLDST Student/home version
ELPLDSI Single user version
ELPLDSL Site licence version

Note that student versions are missing selected exercises and content more applicable to institutions. Student/home version are not available to educational institutions or companies.

System requirements

PC with CD ROM drive and Windows 98 or greater. Site licence version is compatible with all major network configurations.

Hardware requirements

An Altera CPLD or FPGA development system like the E-blocks CPLD solution.