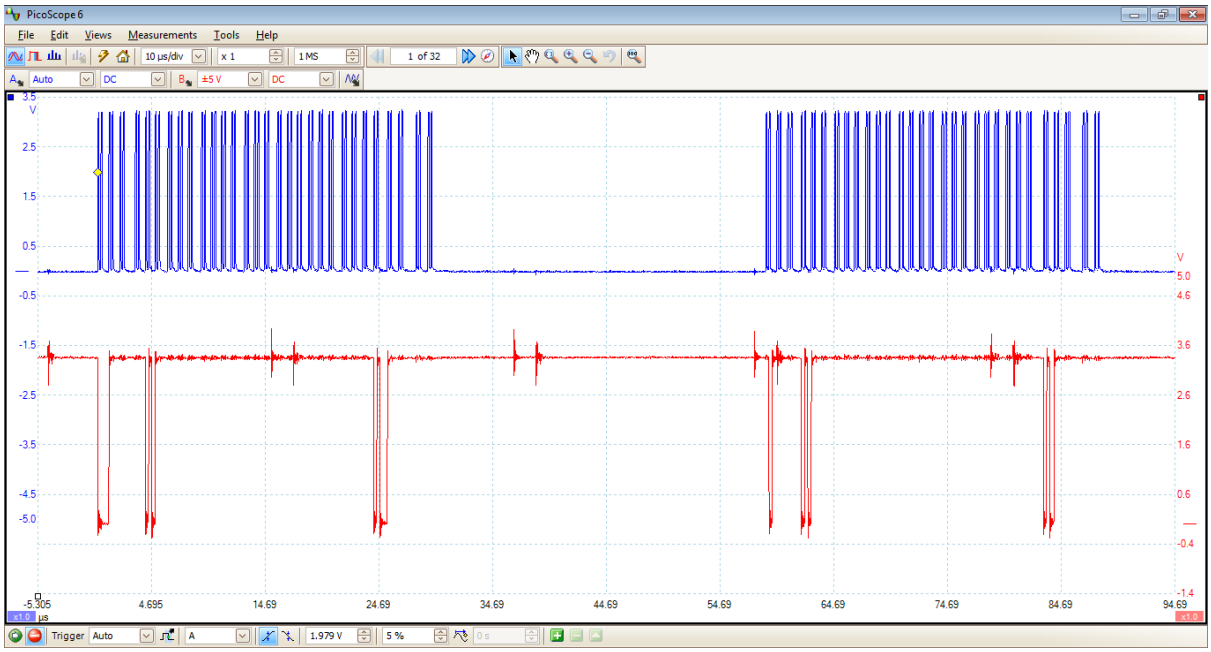

60 data clocks in blue are 28us long to make one line, with pause of 31us before next line starts. (I.e. is like a very long flyback on a CRT.) Data in red is one bit of a 4-bit bus. 59us per line x 240 lines = 14ms per frame = 71Hz refresh rate.

Expansion of above during a line scan:

The 0.25us length data clocks (counting the 1 and the 0) in blue are always in pairs of average period 0.45us (2.2Mhz) not counting above pause between lines when there are no clocks. Gap between each pair of clocks is variable and apparently random in range 0.5 to 1us.

Data in red is one bit of a 4-bit bus. Data is assumed to be read on the falling edge of every clock pulse as that is when data is stable. Data may change in the variable gap between pairs and change

again before new clock falling edge but is presumably not read in the gap as there is no falling edge to read any change then