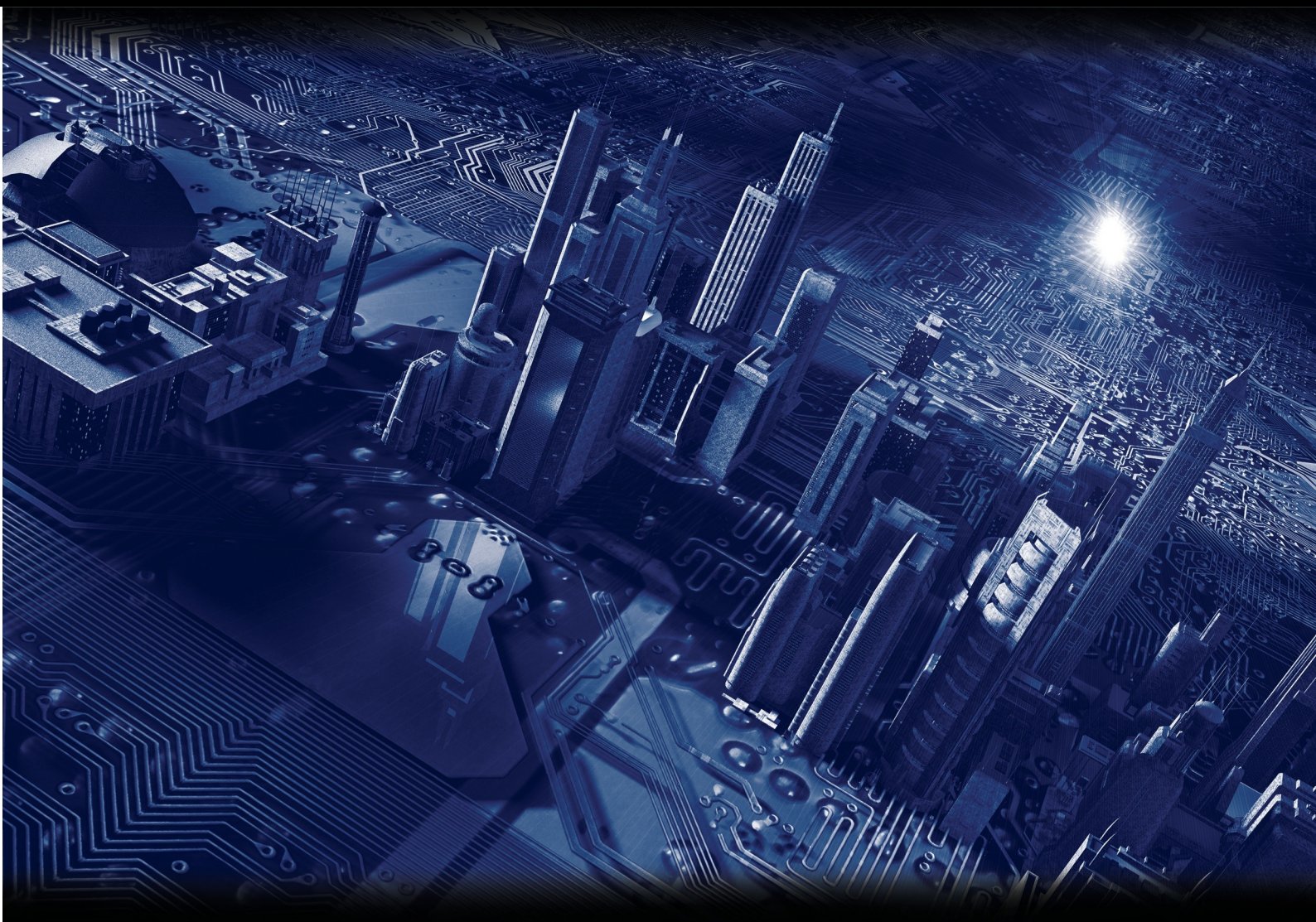
locktronics

Simplifying Electricity

Sequential logic



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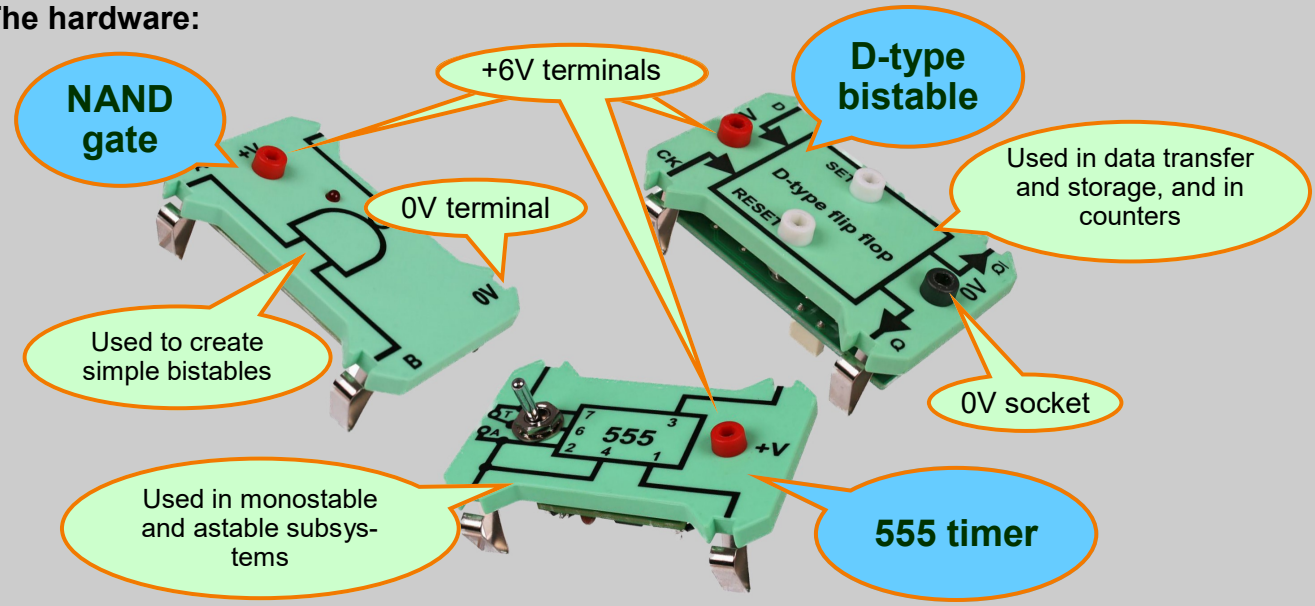
The hardware:



Sequential logic

- In combinational logic, the output depends solely on the state of the inputs at the time.
  - For example:
    - An AND gate outputs a logic 1 signal only while both inputs are at logic 1.
    - A decoder selects the third subsystem when the input signal is 10.
- In sequential logic, as well as the current state of the inputs, the output depends on the sequence of states that led up it.
  - For example:
    - When both inputs are at logic 1, a bistable may output logic 0, or output logic 1, depending on the previous state of the inputs.
    - A counter may have one of a wide range of outputs when its (clock) input goes to logic 1.
- An astable subsystem:
  - has no stable output states;
  - changes the output signal from logic 0 to logic 1 automatically after a set time, and then changes back to logic 0 automatically after a further set time.
- A monostable subsystem:
  - has one stable output state;
  - changes the output signal, from logic 0 to logic 1, say, when triggered by an input signal, and then changes back automatically some time later.
- A bistable subsystem:
  - has two stable output states;
  - changes the output signal from one to the other when triggered, and then changes back when triggered again.

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Introduction

Sequential logic

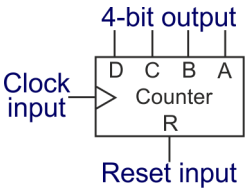
The background:

A monostable sends out a single square pulse when triggered. It is sometimes called a 'one-shot' device. The duration of the pulse depends on component values inside the subsystem, usually a capacitor and a resistor (RC network.)

An astable sends out a continuous stream of pulses. Here again, pulse duration depends on components, usually a RC network, inside the subsystem.
Both monostable and astable subsystems can be built using a 555 timer chip.

A bistable can be used to create a latch, a subsystem that holds the output steady, once triggered, until it receives a second signal, on its Reset input. It is also the basis of a counter. The 'D-type' and the 'J-K' are both bistables.

A counter counts square pulses received at its clock input.
A common format is the 4-bit counter.
The Reset input is used to return the count to zero.



Counting in binary:

Most electronic counters count using the binary number system. This uses only two digits, **0** and **1**. (By comparison, the decimal system uses ten - **0**, **1**, **2**, **3**, **4**, **5**, **6**, **7**, **8** and **9**.)

The table compares these two counting systems.
Notice that the equivalent number in binary contains many more digits. We find it cumbersome to use, but electronic counters work so quickly that they can carry out calculations rapidly using binary.

Decimal	Binary	Decimal	Binary
0	0	8	1000
1	1	9	1001
2	10	10	1010
3	11	11	1011
4	100	12	1100
5	101	13	1101
6	110	14	1110
7	111	15	1111

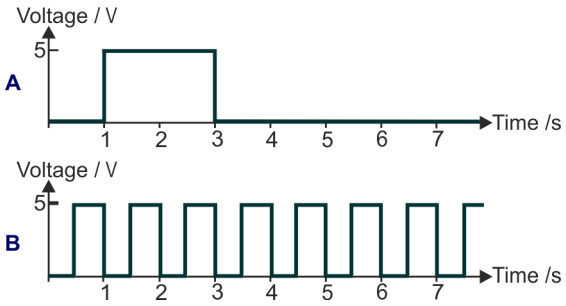
For your records:

Answer the following questions:

- What is the difference between combinational logic and sequential logic?
- Which two of the following are sequential systems?
  OR gate astable bistable counter
- What is the difference between astables, monostables and bistables?

The graphs show two signals, labelled A and B.
Copy them and complete the statements:

Signal ….. shows the output of a monostable system.
Signal ….. shows the output of an astable system.



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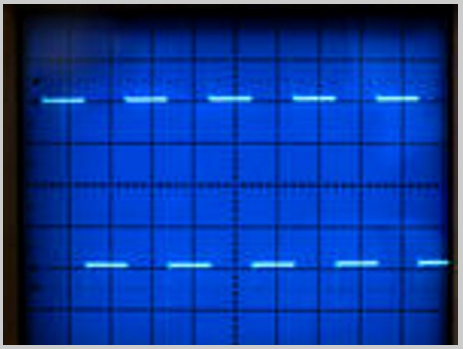
Worksheet 1
The astable

Sequential logic

The astable is the workhorse of sequential logic systems. Also known as ‘oscillator’, ‘astable multivibrator’, ‘flip-flop’ or simply ‘clock’, it generates a series of square pulses used to synchronise the operation of many sequential systems.

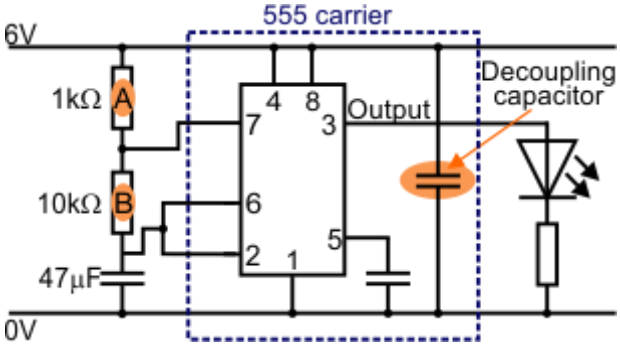
The simplest way to create an astable is to use a ‘555 timer’ chip, first manufactured in the 1970’s. The Locktronics 555 carrier can be switched between astable and monostable modes.

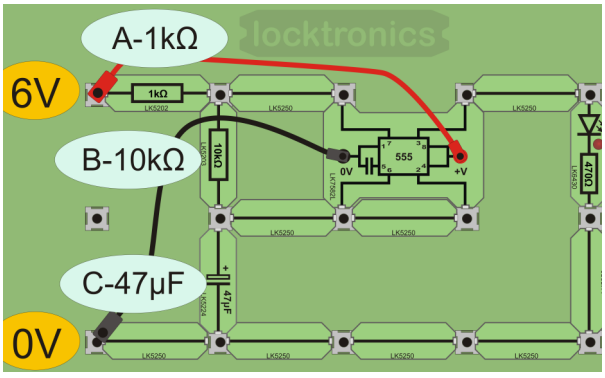


Over to you:

For astable operation, the 555 carrier requires the addition of three ‘timing’ components - two resistors and a capacitor, as shown in the circuit diagram. These control the frequency of the output pulses, and the ‘mark:space’, as explained later on.

- Build the circuit shown opposite.
  - Be sure to connect the 555 carrier to the +6V supply, via the ‘+V’ and ‘0V’ sockets.
- Switch on the 6V power supply.
- The LED connected to the output should be flashing on and off. Time how long it takes to produce ten flashes (i.e. ten ‘on-and-off’s.)
- Enter your measurement in the first row of the table.
- Switch off the power supply. Change the value of resistor ’B’ from 10kΩ to 5kΩ.
- Switch on, and time how long it takes to produce ten flashes now. Enter the result in the second row.
- Repeat this procedure for the other combinations of timing components given in the table.





Timing components			Time for ten flashes
Resistor A	Resistor B	Capacitor	
1kΩ	10kΩ	47µF	
1kΩ	5kΩ	47µF	
1kΩ	5kΩ	100µF	
1kΩ	50kΩ	100µF	

(The circuit diagram for the astable includes a decoupling capacitor. This decouples’ (isolates) the power supply from the oscillations generated by the 555 chip. Without it, small oscillations could appear on the power rails and these could affect other subsystems in the system.)

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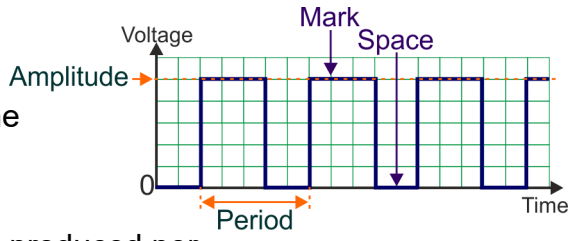
Worksheet 1
The astable

Sequential logic

So what?

Square wave vocabulary:



Amplitude - the maximum voltage in the signal.

Period - the time taken to produce one cycle of the square wave, (i.e. 1 peak plus 1 trough)
- measured in seconds.

Frequency - the number of cycles of the square wave produced per second;
- measured in hertz. (1 Hz means one cycle produced every second.)

These are related by the relationship: ***Frequency = 1 / period***

Mark - the time spent at the peak of the signal.

Space - the time spent at 0V.

Mark:Space - the time the signal sits at its peak, compared with the time at 0V.

- Use your measurements, and the information above, to complete the period and frequency columns in the table.
- From a theoretical analysis, the period T is given by the formula:

$$T = 0.69(R_A + 2 \times R_B) \times C.$$

This formula, and the one above have been used to give calculated values for the first and third sets of timing components. Do the calculations for the other two sets.

Timing components			Measured period in s	Measured frequency in Hz	Calculated period in s	Measured frequency in Hz
Resistor A (R_A)	Resistor B (R_B)	Capacitor (C)				
1kΩ	10kΩ	47μF			0.68	1.47
1kΩ	5kΩ	47μF				
1kΩ	5kΩ	100μF			0.76	1.32
1kΩ	50kΩ	100μF				

A challenge -

When R_B = 100kΩ and C = 100μF, change R_A to 100kΩ.

For your records:

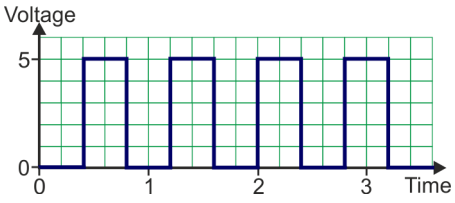
- Copy the circuit diagram for the 555 astable, given near the top of the previous page.
- Copy the signal shown below, and give the information requested.

(a) Amplitude =

(b) Period =

(c) Frequency =

(d) Mark:space =



- Calculate the period and frequency for this astable when the following timing component values are used:

R_A = 5kΩ R_B = 100kΩ C = 22μF

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Worksheet 2
The monostable

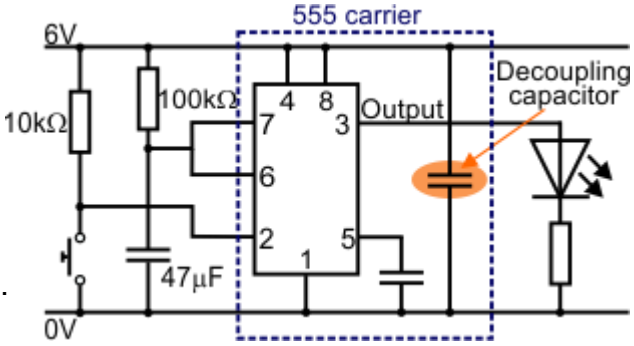
Sequential logic

The monostable subsystem has one stable output state. It remains in it until triggered by an external signal. It then jumps into the other output state. (It is digital, and so has only two possible states.) After a time determined by the timing components, a resistor and a capacitor, it reverts automatically to its stable state.

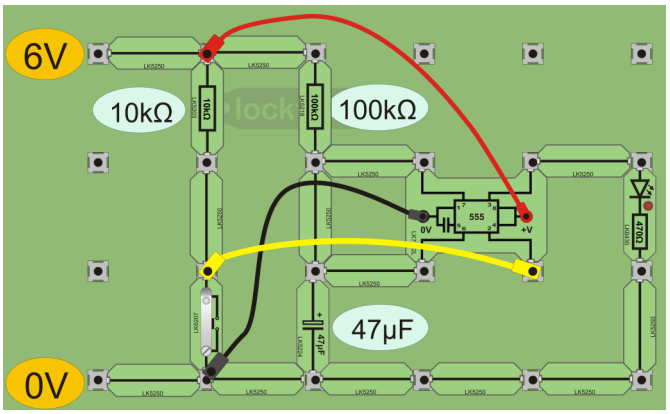
One use is as a time-delay subsystem, used to keep security lights on for a short time once triggered (by a PIR sensor, for example.)

Over to you:

For monostable operation, the 555 carrier requires just two 'timing' components - a resistor and a capacitor, as shown in the circuit diagram.



- Build the circuit shown opposite.
  - Notice the orientation of the switch unit - the 10kΩ resistor is in the 'pull-up' position.
  - Be sure to connect the 555 carrier to the +6V supply, via the '+V' and '0V' sockets.
- Switch on the 6V power supply.
- Press and release the push-switch. The LED connected to the output should come on for a short time and then go off.
- Press it again, and time how long the LED stays lit.
- Enter your measurement in the first row of the table.
- Switch off the power supply.
- Replace the 10kΩ resistor with a 50kΩ resistor.
- Time how long the LED stays on now, and enter the result in the second row of the table.
- Repeat this procedure for the other combinations of components given in the table.



Timing components		Time LED stays lit in seconds
Resistor	Capacitor	
100kΩ	47µF	
50kΩ	47µF	
50kΩ	100µF	
100kΩ	100µF	

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Worksheet 2
The monostable

Sequential logic

So what?

The relationship between the time delay, T, and the timing components is:

T = 1.1 x R x C

Here are the options when using it:

- With R in ohms, and C in farads, T will be in seconds.
- With R in megohms (MΩ), and C in microfarads (μF), T will be in seconds.
- With R in kilohms (kΩ), and C in microfarads (μF), T will be in milliseconds (ms).

Remember:	1kΩ = 1 000Ω
	1MΩ = 1 000 000Ω
	1F = 1 000 000μF

- Using this information, complete the table by calculating the theoretical values of T.

Timing components		1.1xRxC
Resistor	Capacitor	
100kΩ	47μF	
56kΩ	47μF	
56kΩ	100μF	
100kΩ	100μF	

- Compare your results with these theoretical values. Discuss with your colleagues reasons for differences between the theoretical and actual measured values for the time delays.

A challenge - a variation:

Sometimes, a delayed turn on subsystem is needed. In other words, you press the switch, there is a delay and then the device switches on. There are several ways to implement this. Design a system that does this.

Ask your instructor for permission to build and test your solution.

For your records:

- Copy the circuit diagram for the 555 monostable, given on the previous page.
- Copy the formula linking time delay with the values of the timing components.
- Copy and complete these statements about the performance of the monostable subsystem:

  When the value of the resistor is increased, the time delay produced …….. .

  When the value of the capacitor is increased, the time delay produced …….. .

- The formula given above can be re-arranged as:

  R = T / 1.1 x C

  Use this formula to decide what value resistor to use with a 100μF capacitor to produce a time delay of 11 seconds.

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Worksheet 3
The simple bistable

Sequential logic

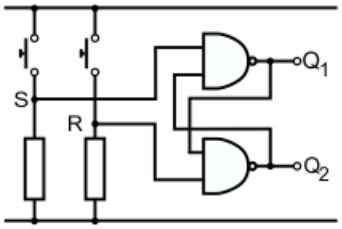
Bistable systems form the basis of electronic memory. Each memory 'cell' is effectively a bistable, storing a single binary digit, either a **0** or a **1**.

The memory modules in the picture each store 8GB of data, which is roughly 8 x 8 x 1000 x 1000000 **0**'s or **1**'s.

That's a lot of bistables!

Over to you:

The significant element in sequential circuits is the use of feedback, where the output signal, or part of it, is sent back to the input.

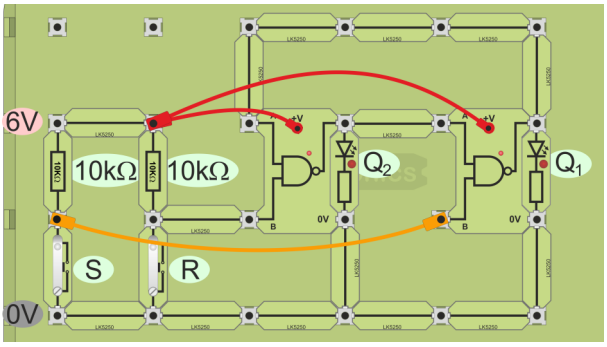


Here, output Q_1 is connected to an input on the lower NAND gate, and Q_2 to an input on the upper gate.
The state of each output is shown on the LED carrier attached to it. When the LED is lit, the output is logic 1, when not lit, logic 0.

- Build the circuit shown opposite.

  Notice the orientation of the switch units - they use pull-up resistors to keep the inputs of the gates at logic 1 until the switch is pressed.

  When a switch is pressed, the switch unit sends a logic 0 signal to the gate input.
  (You can show this by adding LED carriers between the 'B' inputs and 0V.)



- Switch on the 6V power supply. The system starts in any state. Complete the first row of the table with the initial states of Q_1 and Q_2 (before any switches are pressed.)
- Now press switch 'S' , to input a logic 0 signal. Use the LEDs to identify the logic states of outputs Q_1 and Q_2 and record them in the second row of the table.
- Release switch 'S' , so that both 'S' and 'R' inputs are at logic 1. Record the outputs states in the third row.
- Continue in this way to complete the table.

S (Set)	R (Reset)	Q_1	Q_2
1	1		
0	1		
1	1		
1	0		
1	1		
0	1		
1	1		
1	0		
0	0		

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Worksheet 3
The simple bistable

Sequential logic

So what?

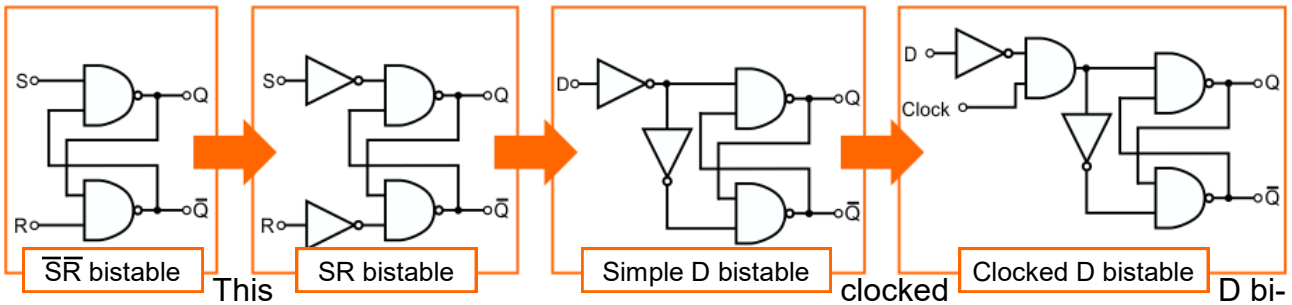
- Rows 1,3,5 and 7 - Setting both inputs to logic 1 does not fix the state of the outputs! Sometimes $Q_1 = 0$, $Q_2 = 1$ and sometimes it is the other way round. It depends on what happened previously - it just preserves the previous states of the outputs.
- Rows 2 and 6 - Whenever, 'S' is logic 0, Q_1 is logic 1 (set). Hence the label 'S' for the switch.
- Rows 4 and 8 - Whenever, 'R' is logic 0, Q_1 is logic 0 (reset). Hence the other switch is 'R'.

So far everything is civilised - Q_1 and Q_2 sit in opposite states.
As a result, the outputs are normally known as **Q** and **Q.** The inputs are 'active low', meaning that they cause changes when they are 'low', logic 0, and so this is known as a ~~SR~~ bistable.

A problem - row 9! The outputs are not opposites - both are at logic 1. The new names fail!

The shortcomings of the basic bistable are overcome through a series of modifications.

1. *Illogical! - to make the output logic 1, input a logic 0!*
   Add NOT gates to each input, making them 'active high'. (S = 1, R = 1 is now the forbidden combination.) This is now the SR bistable.
2. *There is still a forbidden combination!*
   Connect a NOT gate between the 'S' and 'R' inputs. Now the two inputs cannot be the same. We have only one input, however, the D (data) input. It is the simple D bistable. Whenever D =1, Q = 1 ($\overline{Q}$ = 0). Whenever D = 0, Q = 0 ($\overline{Q}$ = 1).
3. *The outputs are not protected. Whenever the input changes, the output changes!*
   Add an AND gate. The second input is called the clock input. The outputs can change now only when the clock input is raised to logic 1. This is the clocked D bistable.



This clocked D bistable is 'level-triggered' - the output can change whenever the clock input is at logic 1. The commercial D-type bistable has 'edge triggering' added.
This is the focus of worksheet 4.

For your records:

- Copy the circuit diagram for the $\overline{S}\overline{R}$ bistable, given near the top of the previous page.
- Why are the outputs known as Q and $\overline{Q}$? Why are the inputs called $\overline{S}$ and $\overline{R}$?
- Describe three problems associated with this bistable, and a modification that will cure each. Include the circuit diagram for each modification with your explanation.

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Worksheet 4
The D-type bistable

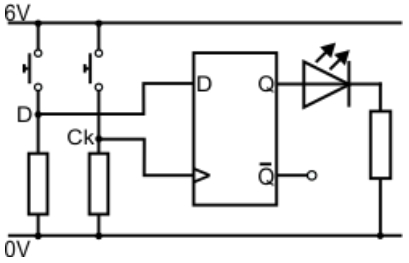
Sequential logic

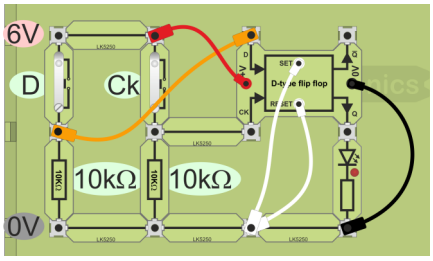
One use of a D-type bistable is to create an electronic latch - a subsystem which, once triggered, stays on until a reset signal is received.
An alarm, such as a car alarm, uses this approach.
When someone breaks in, the alarm sounds until the car owner turns it off, often by pressing a switch on the remote control fob.

Over to you:

1 - D-type principles:

- Set up the circuit shown opposite. We are not using the 'Set' and 'Reset' inputs here, so they are connected to 0V.
- Switch on the 6V power supply.
  If the LED is lit, press and release the 'Ck' switch.
- Now work through the sequence that follows, completing the table with the state of the LED each time:
  (a) Press and hold down the 'D' switch.
  (b) Now press, hold down and release the 'Ck' switch.
  (c) Release the 'D' switch.
  (d) Press, hold down and release the 'Ck' switch again.



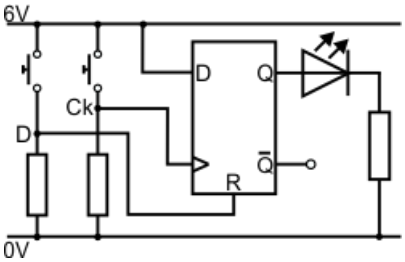


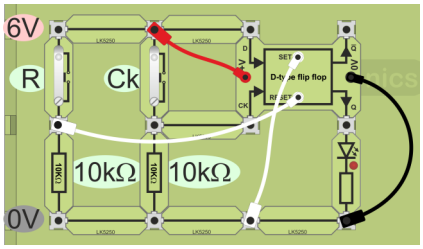
Step	'D' switch	'Ck' switch	LED
(a)	On	Off	
(b)	On	On / Off	
(c)	Off	Off	
(d)	Off	On / Off	

- With the circuit in front of you, answer Q1 in the 'For your records' section.

2 - The latch:

- Modify the circuit as shown.
  - The 'D' input is connected directly to +6V.
  - The left-hand switch unit controls the 'Reset' input on the D-type bistable carrier.
  - 'Set' is still not used, and remains connected to 0V.
- Observe what happens when you:
  (a) Press and then release the 'Ck' switch.
  (b) Press and release the 'R' switch.
- Use these observations to answer Q2 in the 'For your records' section.





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Worksheet 4
The D-type bistable

Sequential logic

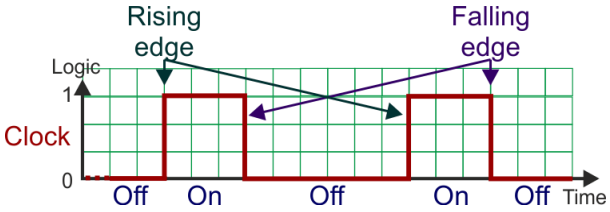
So what?

1 - D-type principles:

Switch behaviour:

- Switch off - the 'pull-down' resistor, between the input and 0V, holds the input at logic 0.
- Switch on - the input is connected to +6V, inputting a logic 1 signal.

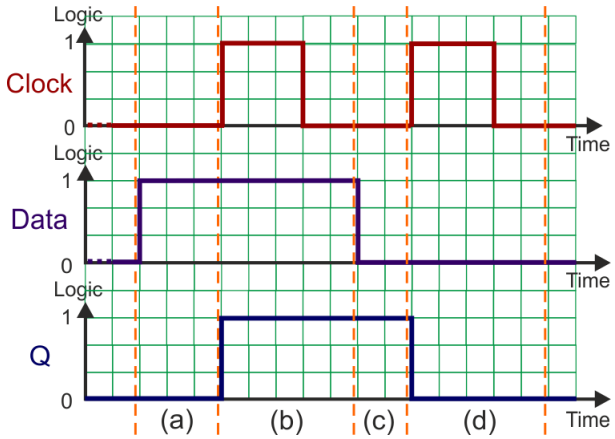
This behaviour is shown in the first timing diagram.



D-type bistable behaviour:

- The bistable is 'rising-edge' triggered. (The first timing diagram illustrates the meaning of 'rising-edge' and 'falling-edge'.)
- On the rising-edge of a clock pulse, the Q output of the D-type copies the logic level present on the D input of the bistable.

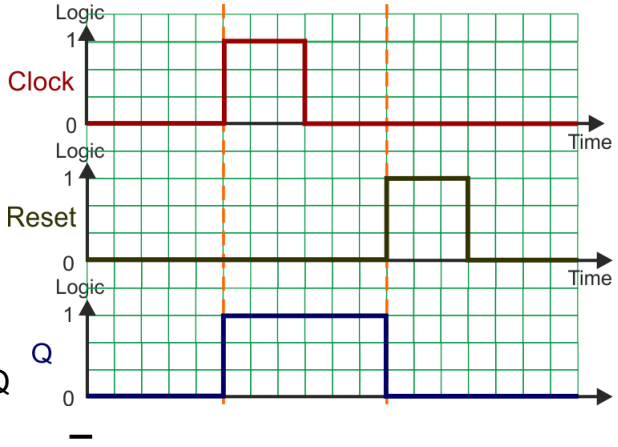
The timing diagram opposite is one way to express your observations from parts (a) to (d) earlier.
Check that you understand and agree with it!



2 - D-type latch behaviour:

Now, the Data input ('D') is permanently connected to logic 1, (+6V).

- On the first rising-edge of the clock pulse, the Q output copies it and goes to logic 1.
- When the Reset input goes high, however, the Q output is reset to logic 0.



A challenge -
Add a second LED carrier to show the state of the Q output in the two circuits.
Add a new graph to the two timing diagrams to show your results.

For your records:

- Answer the following questions:
  1. In the first circuit, what is the purpose of the 'D' switch and of the 'Ck' switch?
  2. What is the meaning of 'latch'?
     (Use your observations of the second circuit in your answer.)
- Copy the three timing diagrams.
  Add labels to each to explain what is happening at different stages.

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Worksheet 5
The 1-bit counter

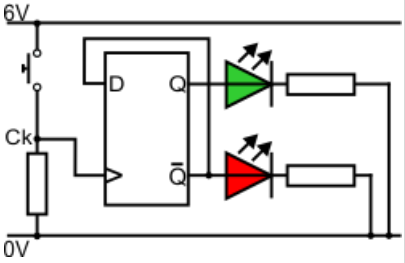
Sequential logic

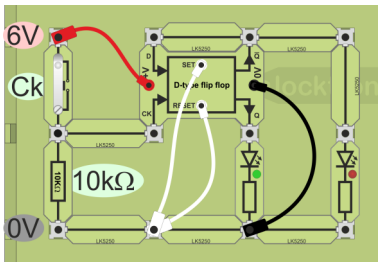
Electronic counting systems have countless uses in our lives. They count people entering lifts, or train carriages, count eggs in a packing factory, count coins in a bank, pills dispensed to pharmacies and even count votes in political elections.
They count using the binary number system, discussed in the Introduction, but may display the result in decimal numbers, more understandable to humans.
This worksheet looks at the basic unit of counters, the 1-bit counter.

Over to you:

1 - One-bit counter

- Set up the circuit shown. Notice that the Data input is connected to the $\overline{Q}$ output. A second LED carrier shows the state of the $\overline{Q}$ output.
- Switch on the 6V power supply. If the LED is lit, press the 'Ck' switch once.
- Press and release the 'Ck' switch a number of times, to send in clock pulses and observe the effect on the LED.
- Record your results in the table that follows.

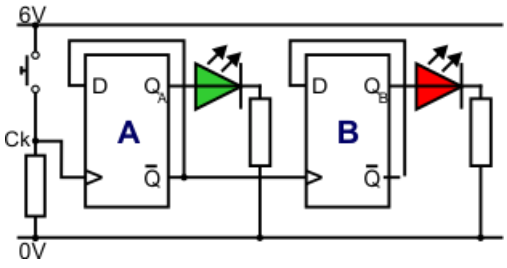


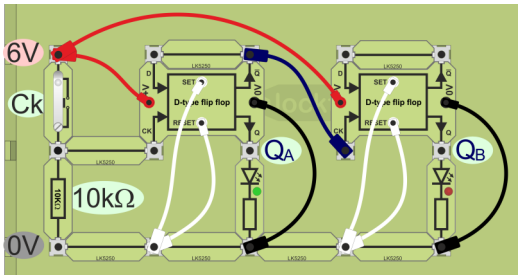


Clock pulse	State of LED
0	Off
1	
2	
3	
4	
5	

2 - Two-bit counter

- Add a second D-type bistable, as shown. Again, the Data input is connected to the Q output. The red LED now shows the state of the second bistable output.
- Switch on the 6V power supply. If any LED is lit, press the 'Ck' switch until both are off.
- Generate clock pulses, as before and watch the effect on the two LEDs.
- Record your results in the table that follows.





Clock pulse	Q_A	Q_B
0	Off	Off
1		
2		
3		
4		
5		

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Worksheet 5
The 1-bit counter

Sequential logic

So what?

The nub of this behaviour is the connection between $\bar{Q}$ and the Data input.

The sequence of events, illustrated in the table, is:

- $\bar{Q}$ is always in the opposite state to Q.
- $\bar{Q}$ is connected to the Data input.
- Hence the Data input is always in the opposite state to Q.
- On the next clock pulse, Q copies D and moves to the opposite state.

Clock pulse	Q output	$\bar{Q}$ output	Data input
1	0	1	1
2	1	0	0
3	0	1	1
4	1	0	0
5	0	1	1
6	1	0	0

The table opposite repeats the comparison of binary and decimal number systems, with the binary numbers written over four columns.
For example, '5' = '0101'

Look at the 'A' column.
It follows the same pattern as the Q output of the bistable. As a result, this subsystem can be called a 1-bit counter.

Decimal number	Equivalent binary number DCBA			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

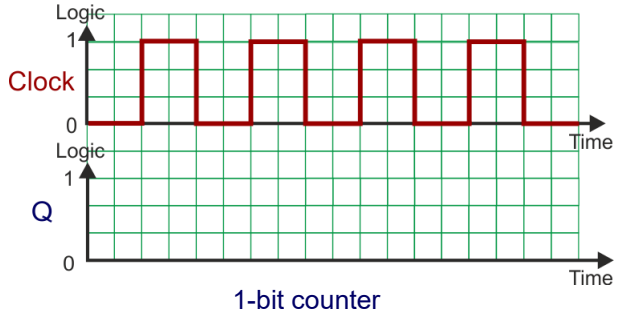
In circuit 2, the second bistable acts in the same way as the first. The Q output changes state every time it receives a clock pulse. However, here, the Q output of the first bistable provides these clock pulses. As your results show, it takes two pulses from the switch to
create one of these clock pulses. In other words, its behaviour looks like column B of the table above. In summary, this circuit behaves as a 2-bit binary counter.

A challenge -

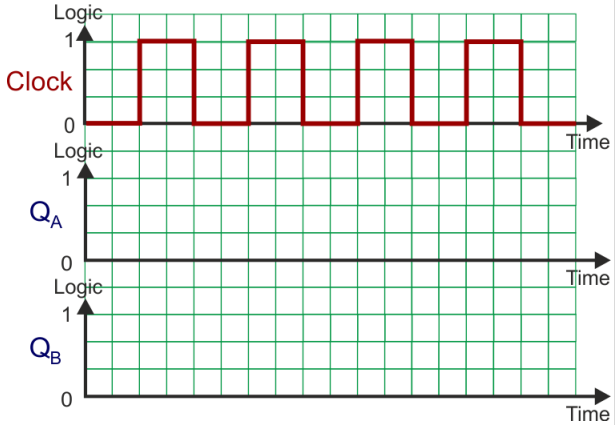
Modify the 2-bit counter so that the second bistable receives clock pulses from the Q, not $\bar{Q}$, output of the first. Spot the difference!

For your records:

- Copy the circuit diagrams and test results for the 1-bit and 2-bit counters.
- Use your results to complete the timing diagrams given below.



1-bit counter



2-bit counter

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Worksheet 6
Debouncing with a monostable

Sequential logic

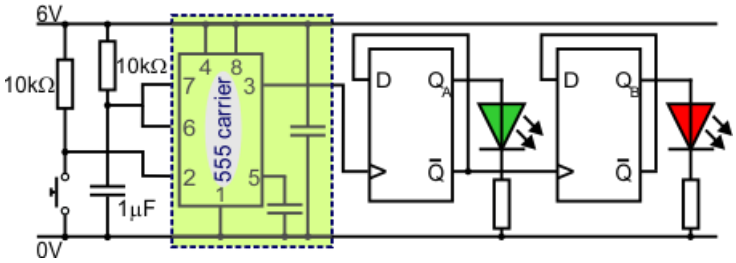
Counting the number of times a switch is pressed poses a significant problem - switch bounce.

Switches are designed using springy materials - brass, steel etc.
A switch must close quickly, to avoid 'arcing'.
In the process, the two metal contacts come together very quickly - and often bounce off again, and again.
What is meant to be one press of the switch looks to the electronics as a number of presses.

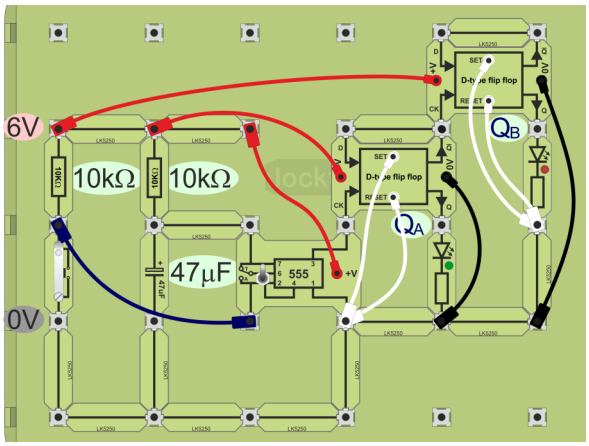
The solution is to add a debouncing circuit, to remove the surplus pulses. As these worksheets shows, there are a number of ways to do this.

Over to you:

- Set up the circuit shown. Notice that $\overline{Q}_A$ is connected to the clock input of the second D-type bistable. In other words, it is connected to count up.
- Switch on the 6V power supply.
- Press and release the switch a number of times, (roughly once per second).
- Observe the effect on the LEDs.
- Use the table to record what you see.



Clock pulse	Q_A	Q_B
0	Off	Off
1		
2		
3		
4		
5		



- The aim is to eliminate switch bounce.
  The proof is a results table that shows an unbroken and correct sequence of outputs.
- Optimise the time delay using different values of timing components. Make a note of the optimum values for your system.
- Another source of unwanted pulses is noise on the power rails. This can be reduced by connecting a large value capacitor between the +6V rail and 0V.
  Try this out, but ***be very careful to connect the capacitor the right way round***, if it is an electrolytic capacitor. The positive electrode must be connected to the +6V power rail, and the negative electrode to 0V.

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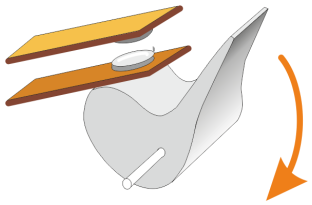
Worksheet 6
Debouncing with a monostable

Sequential logic

So what?

The monostable as a debouncing subsystem:



The diagram illustrates the inner working of a switch.
It has two springy metal contacts.

- When the switch is off, they are not touching.
- When it is turned on, they are forced together.

The changeover must be rapid, as otherwise prolonged sparking can occur when the contacts are almost touching, which will cause wear and corrosion, reducing the lifetime of the switch.

However, as the contacts are springy, this rapid closing can cause them to bounce open again, and bounce several times before finally coming to rest in the closed position. This creates false pulses in a counting system.

You probably observed this in the previous worksheet, where the sequence of output states sometimes jumped one or more states. The first method for tackling the problem is to add a monostable, set up to create a very short delay. For the circuit shown on the previous page, the formula $T = 1.1 \times R \times C$ predicts a delay of 11ms.

During this time, the output of the monostable remains steadily at logic 1, no matter how many times the clock input bounces up and down. Providing all switch bounces cease before the output falls to logic 0, this method will debounce the switch.

The disadvantage of this method is that the counter might miss pulses if they arrive with a very short time interval between them. This is where the need to optimise the time delay is important. A long delay means that it is very unlikely that switch bounce will be a problem, but the system is insensitive during that delay.

Electrical noise contains a range of high frequencies. Capacitors offer very little impediment to high frequencies, but block low frequencies. A capacitor connected between the power rails offers an easy route to these high frequencies, effectively reducing their effect on the rest of the system.

For your records:

- Copy the circuit diagram for the system, showing the use of the monostable to debounce the switch.
- Add your best set of timing component values to the diagram.
- Explain the principle behind the method, in terms that one of your fellow students would understand.
- Explain how to reduce noise in power rails, using a decoupling capacitor.

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Worksheet 7
Debouncing with a bistable

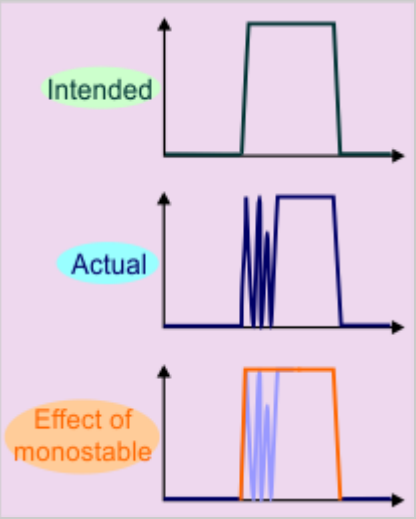
Sequential logic

The previous worksheet showed that a monostable subsystem can mask the unwanted pulses produced by switch bounce.

The diagram illustrates this principle. The monostable output, (orange,) stays high until the bouncing has stopped. Overall, the counting system receives a single pulse, just as intended.

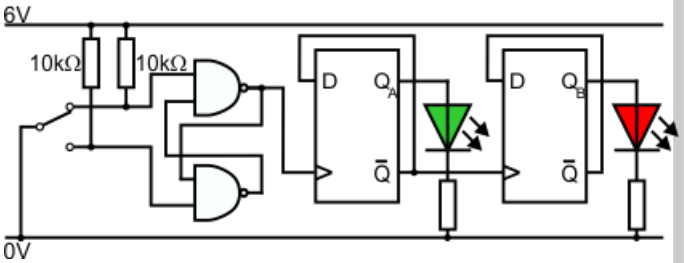
There are side-effects! The counter may not see some valid pulses, or may see spurious pulses created in the power supply.

The next solution has none of these disadvantages. It relies on the latching property of a bistable.



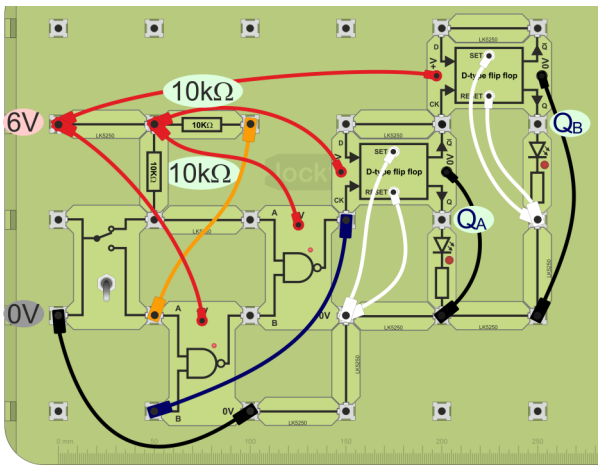
Over to you:

- Set up the circuit shown.
  Once again, $\overline{Q}_A$ delivers clock pulses to the second bistable, to make it count up.
- Switch on the 6V power supply.
- Move the switch from one position to the other and observe the LEDs as you do so.
- Continue until both LEDs are off, (i.e. Q_A and Q_B are both at logic 0.)



- Now operate the switch five times, to send in five clock pulses. Observe the state of the LEDs attached to QA and QB as you do so.
- Complete the table with your results.

Clock pulse	Q_A	Q_B
0	Off	Off
1		
2		
3		
4		
5		



- The operation of this system should be flawless.

The main drawback is its dependence on a single-pole-double-throw switch, which is fine for this application, but not always suitable when using other sensing subsystems.

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Worksheet 7
Debouncing with a bistable

Sequential logic

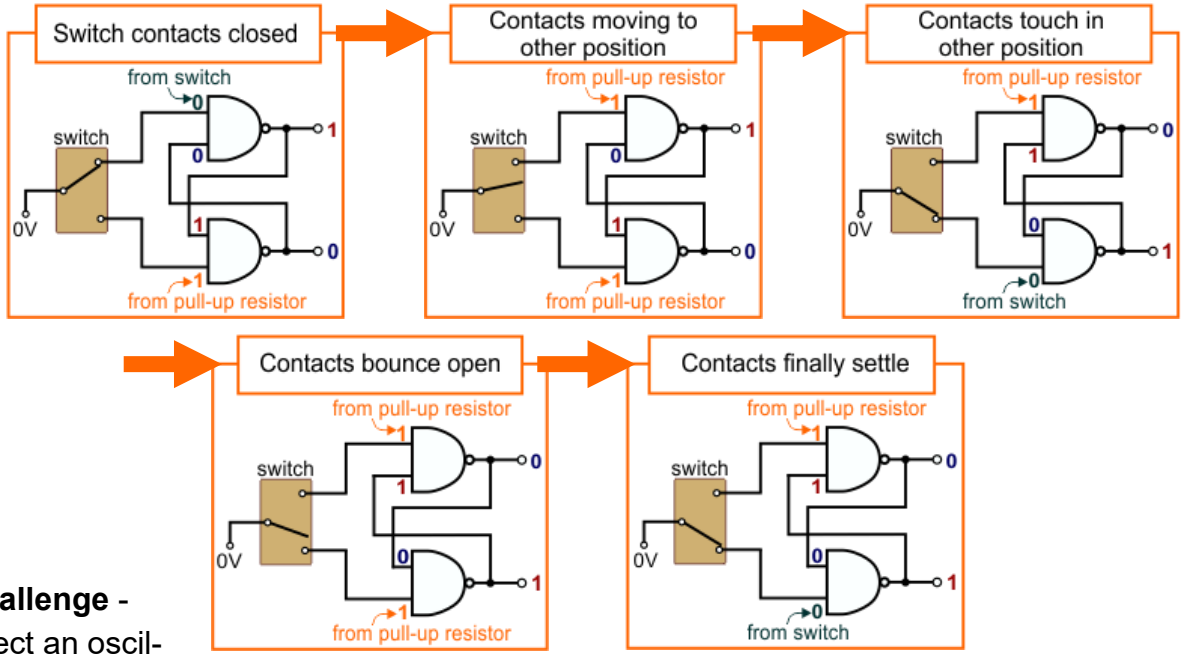
So what?

The bistable as a debouncing subsystem:

You may need to look back at worksheet 3 to appreciate how debouncing works here.

- When the switch contacts are closed, one of the NAND gate inputs is connected to 0V, (logic 0). As a result, the output of that NAND gate is logic 1.
- When the switch is moved to the other position, the contacts separate. No NAND gate is connected to 0V. Instead, the 10kΩ pull-up resistors hold both inputs at logic 1. This is the latching condition, and the output of the gates does not change.
- When the switch contacts meet again, the other NAND gate input is connected to logic 0, and its output goes to logic 1. The contacts may bounce open again, making both inputs return to logic 1, but the outputs do not change. This is the debouncing action.

This sequence is illustrated in the following diagrams.



A challenge -

Connect an oscilloscope to the output of a switch unit, to obtain a trace showing contact bounce. Suggested settings for the oscilloscope are:

Timebase = 1ms/div. Voltage sensitivity = 1V/div

For your records:

- Copy the circuit diagram for the system, showing the use of the bistable to debounce the switch.
- Explain the principle behind the method to one of your fellow students, and then ask her/him to explain it back to you to test understanding.

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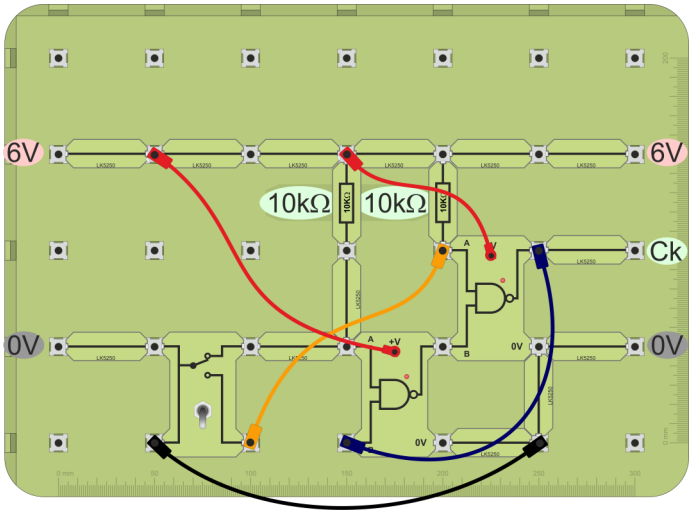
Worksheet 7A
The bistable debouncer

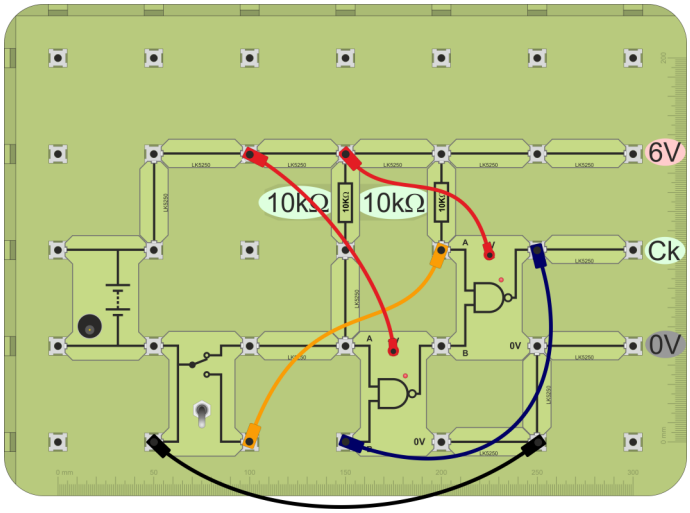
Sequential logic

The next three worksheets require a reliable debounced switch. To streamline the process, you are going to assemble one on a separate baseboard, which you can then connect to other subsystems, in the following worksheets.

Over to you:

- Set up one of the debouncing circuits shown below. The second one is for plug-top power supply users.
- To test it:
  - connect a LED carrier between the ‘Ck’ output and 0V;
  - operate the switch a number of times;
  - check the performance with that seen in the previous worksheet.





- Leave it assembled so that you can use it with the subsystems described in the following three worksheets.

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Worksheet 8
The 3 bit counter

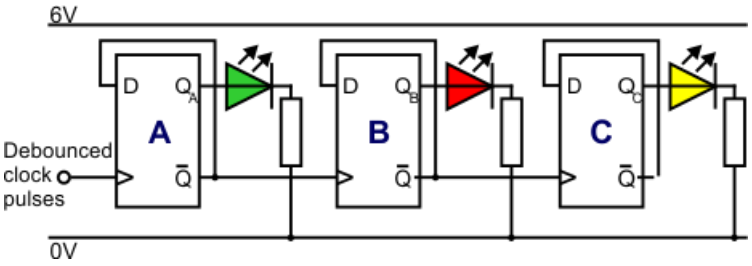
Sequential logic

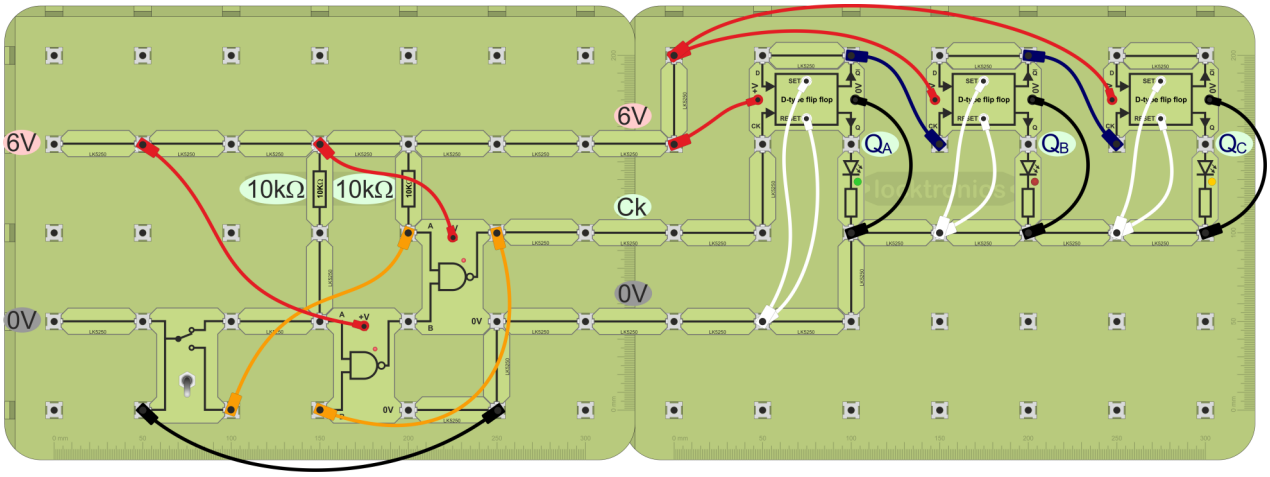
Worksheet 5 studied a 2-bit counter, built from D-type bistables. This one adds a third counting stage, and the next develops it into the 'modulo-n' counter, which resets on the 'n^{th}' clock pulse.

This worksheet shows that the performance of the counter depends on where you take the clock pulse from.

Over to you:

- Build the three-bit counter, and attach the debounced switch baseboard. Again, the $\overline{Q}$ outputs deliver clock pulses to the next stage, to make the system count up.





- Switch on the 6V power supply.
- Use the debounced switch to generate clock pulses and observe the effect on the LEDs.
- Continue until all three LEDs are off, (i.e. Q_A,Q_B and Q_C are both at logic 0.)
- Now operate the switch ten times, to create ten clock pulses. Observe the output LEDs as you do so.
- Complete the table with your results.

Clock pulse	Q_A	Q_B	Q_C
0	Off	Off	Off
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			

- **Do not dismantle this circuit!**
  It forms the basis for the modulo-n counter on the next worksheet.

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Worksheet 8
The 3 bit counter

Sequential logic

So what?

- First of all, convert your results showing whether the LEDs were on or off into logic levels. Remember - when an LED is lit, the output connected to it is at logic 1.

Clock pulse	Q_A	Q_B	Q_C
0	0	0	0
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			

- Compare your results with the table, given in the introduction, which relates the binary and decimal number systems.

Decimal	Binary	Decimal	Binary
0	0	8	1000
1	1	9	1001
2	10	10	1010
3	11	11	1011
4	100	12	1100
5	101	13	1101
6	110	14	1110
7	111	15	1111

A challenge -

Re-arrange the wiring so that the Q outputs, not $\overline{Q}$ outputs, provide clock pulses for the following bistable.

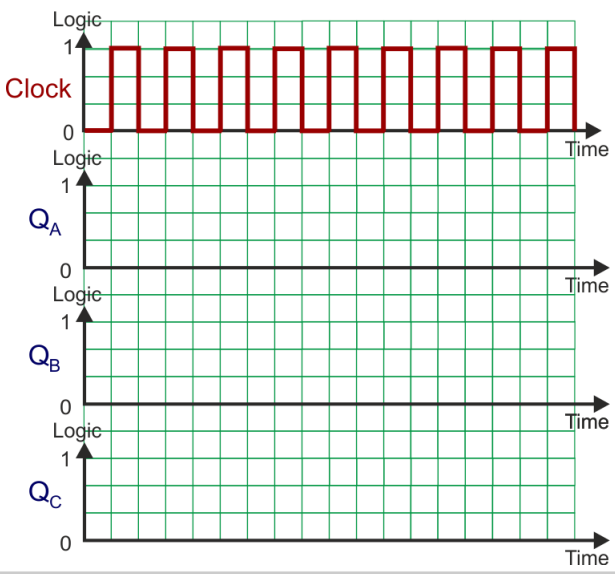
What effect does this have on the performance of the counting system?

For your records:

- Copy the circuit diagrams and test results for the 3-bit counter.
- Copy and complete the sentence:

  The biggest number, in decimal, that this counter reaches is ……. .
- Use your results to complete the timing diagram given opposite.
- Draw the circuit diagram for a 4-bit up-counter based on D-type bistables.
- Copy and complete the sentence:

  The biggest number, in decimal, that a 4-bit counter can reach is ……. .



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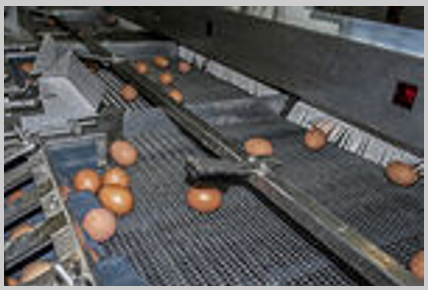
Worksheet 9
The ‘modulo-n’ counter

Sequential logic

Worksheet 5 studied a 2-bit counter. Worksheet 8 added a third counting stage. This one creates a ‘modulo-n’ counter, which resets on the ‘nth’ clock pulse. The 7-segment display is added to show the count as a decimal number.

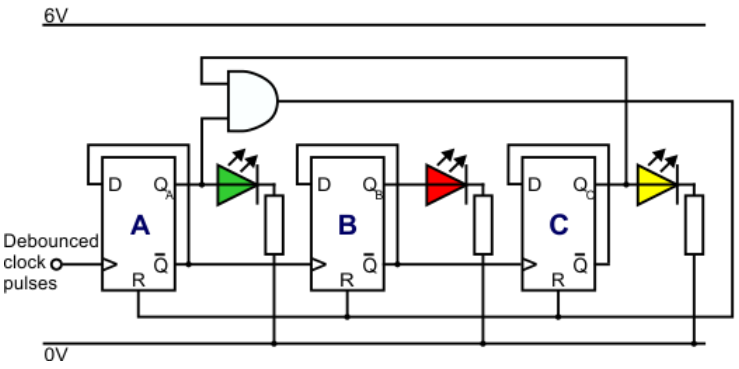


The 3-bit counter resets once a particular number is reached. This is used in applications where a maximum count is required. For example, when packing eggs, the counter may need to reset on reaching ‘6’ (known as a ‘modulo-7’ counter). The system closes the box and starts again.

Over to you:

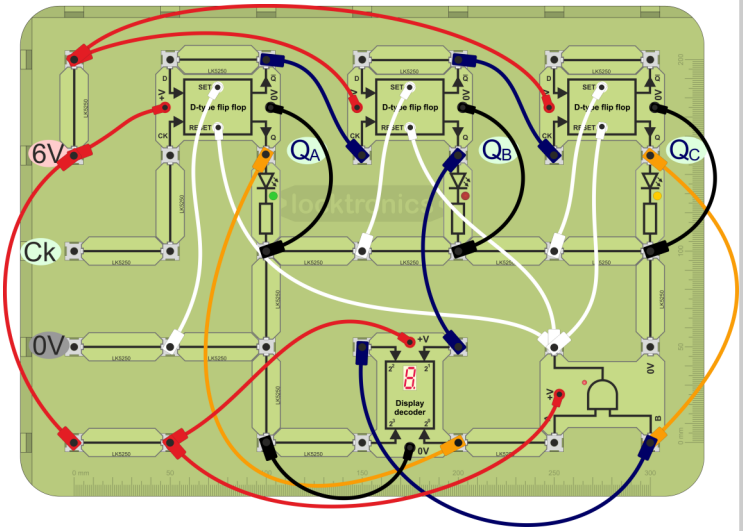
Set up the circuit including the debounced switch baseboard to deliver clock pulses via the ‘Ck’ connection. (The circuit from the previous worksheet, can be modified by adding the AND gate, and 7-segment display.)

- The procedure is the same as in worksheet 8. Switch on the 6V power supply.
- Use the switch on the debounced switch baseboard to generate clock pulses and observe the LEDs as you do so.
- Continue until all three LEDs are off.
- Now operate the switch ten times, to send in ten clock pulses. Observe the state of the outputs LEDs as you do so.



- Complete the table with your results.

Clock pulse	Q_A	Q_B	Q_C	Display
0	Off	Off	Off	**0**
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				



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Worksheet 9
The 'modulo-n' counter

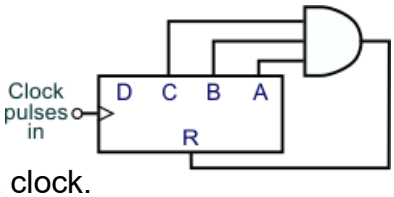
Sequential logic

So what?

- As before, convert your results into logic levels. ('Off' = '0', 'On' = '1'.)
- Compare them with the results for worksheet 8. There, the maximum binary number was '111', on the seventh clock pulse. The counter then reset on the eighth pulse.
- This system relies on the 'Reset' inputs, which reset the bistable (make the Q output logic 0,) when a logic 1 signal is sent to the Reset input.
- On your system, the Reset inputs of all three bistables connect to the output of a 2-input AND gate.
  Its input signals come from Q_A and Q_C. As a result, they reset when Q_A = 1 AND Q_C = 1, i.e. on the fifth clock pulse. The reset process takes only microseconds and so we do not see this state on the LEDs. Instead, the LEDs turn off.
- In electronics jargon, it is a modulo-5 counter:
  - It resets on the 5th clock pulse.
  - The outputs have 5 possible states - 000, 001, 010, 011, 100.
    (Notice - the biggest is '4' in decimal, because '0' is included as one of the 5 states.)

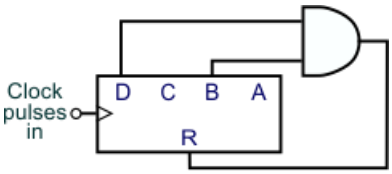
Clock pulse	Q_A	Q_B	Q_C	Display
0	0	0	0	**0**
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

The counter can be contained within a single chip. The diagram shows a 4-bit counter, connected to a 3-bit AND gate as a modulo-7 counter. The biggest number it outputs is '110' ('6' in decimal,) making it suitable for an electronic dice, or the 'tens of minutes' digit in a clock.



For your records:

- Copy and complete the statement:
  A modulo-5 counter resets on the …..th clock pulse, and outputs numbers up to ... .
- Copy the diagram and complete the statements:
  The diagram shows s modulo-….. counter.
  The biggest number it outputs is ….. .



- Copy the diagram for the modulo-7 counter, given above, and explain why it is suitable for the 'tens of minutes' display in an electronic clock.

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Worksheet 10
The 3 stage shift register

Sequential logic

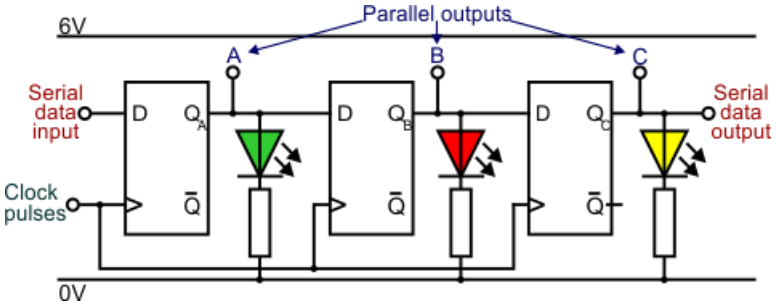
In electronics, the word ‘register’ often means a data store, a location where a binary number can be saved for later use.

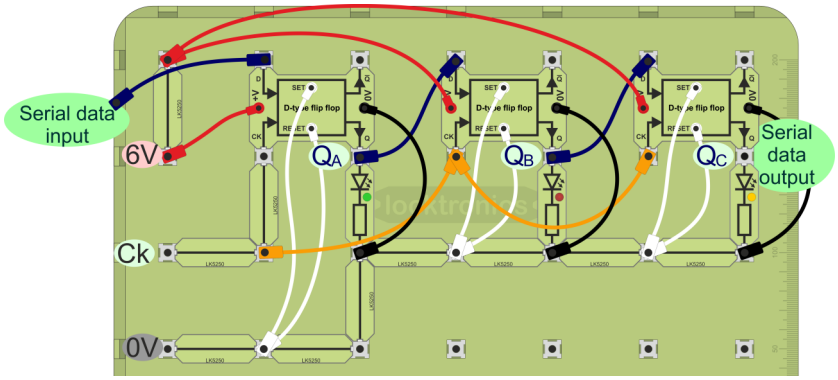
Electronic memory is an array of these registers. Questions that arise include “How do I find it again later?” and “How big a number can I store?”

This worksheet begins that study with a look at how a series of bistables can be used to store data, and how that data can be shifted in a and out of that register.

Over to you:

- Set up the shift register circuit, and attach the debounced switch baseboard to deliver clock pulses via the ‘Ck’ connection.
- Connect the serial data input to 6V (logic 1).
- Switch on the 6V power supply.
- Use the debounced switch to generate clock pulses and observe the LEDs as you do so.
- Once all three LEDs are on, connect the serial data input to 0V (logic 0).
- Now send in further clock pulses, and notice the effect on the LEDs.
- By changing the serial data input connection, store the number ‘101’ in the shift register. It will stay there indefinitely as long as the power supply remains active, and providing no further clock pulses are applied to the input.





- The stored data is extracted from the serial data output, by sending in sufficient clock pulses, in this case three.

Notice the differences between the counter and shift register circuits:

- clock pulses from the debounced switch are fed to all bistables simultaneously;
- the Data input of each bistable is connected to the previous Q output, not $\bar{Q}$ output.

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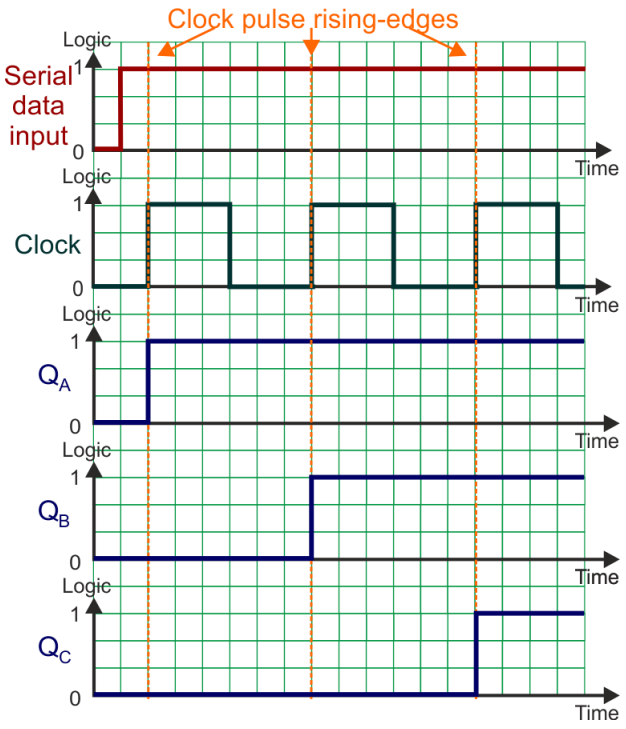
Worksheet 10
The 3 stage shift register

Sequential logic

So what?

- Each D-type bistable copies the state of its Data input to its Q output on the rising-edge of a clock pulse.
- Here, apart from the first bistable, each Data input is connected to the previous Q output.
- The combined effect is that the data bit applied
  at the Data input of the first bistable is passed along to the following bistables, one step at a time, by sending in a series of clock pulses.
- To load a 8-bit number, it is applied in serial fashion, i.e. one bit at a time, to the first Data input, and then eight clock pulses move the data to the eight bistables needed to store it.
- A further eight clock pulses will push the data out of the serial data output.



- The timing diagram opposite shows this. To make this more understandable, remember that changes in the outputs occur extremely rapidly. It may work better to think that the Q output of each bistable copies the data input logic level *just before* the rising-edge of the clock pulse.

Types of shift register:

The circuit you built allowed data to be fed in, one bit at a time, via the serial data input. Eventually, that data could be extracted from the serial data output. This is known as a 'serial-in-serial-out' (SISO) shift register.

However, once the data is stored as described above, it can be extracted simultaneously from each Q output. This is a 'serial-in-parallel-out' (SIPO) shift register.

Other variations allow all data bits to be inserted and extracted simultaneously - a 'parallel-in-parallel-out' (PIPO) shift register, or inserted simultaneously, but extracted one bit at a time from the serial data output - a 'parallel-in-serial-out' (PISO) shift register.

For your records:

- Copy the circuit diagram for the shift register given on the previous page.
- Write a bullet list of the steps needed to store the number '101' in this shift register.
- Draw a timing diagram for the process you just described.
- Describe the differences between SISO, SIPO, PISO and PIPO shift registers.

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Worksheet 11
The R-2R DAC

Sequential logic

Digital processing has a number of advantages:

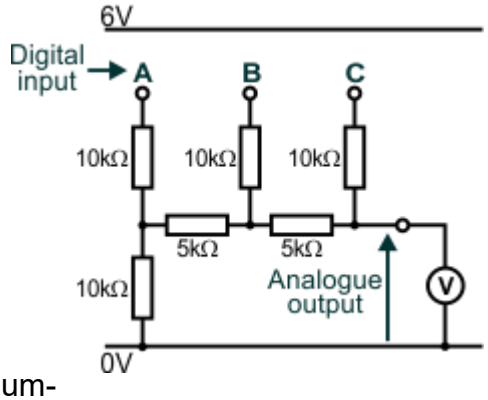
- regeneration - errors and noise can be eliminated;
- added functionality - effects like compression and encryption;
- increased security.

Audio signal processing has embraced digital technology in the form of CDs, DVDs and media streaming over the internet.

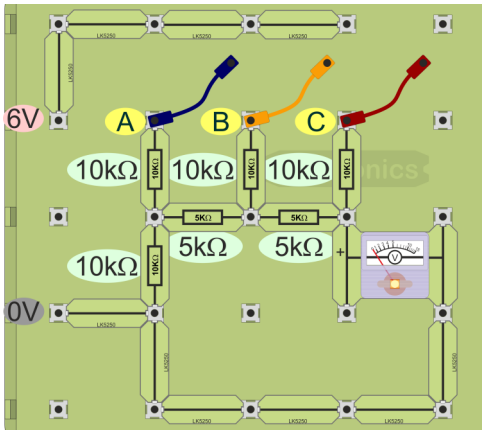
However, ultimately, our ears are analogue devices and so digital audio signals must be converted into analogue signals, if we are to hear them correctly. This requires a digital-to-analogue converter (DAC).

There are a number of ways to implement the DAC circuit. This worksheet looks at one known as the R-2R ladder.

Over to you:



- Set up the circuit, leaving inputs **A**, **B** and **C** unconnected.
- The input, the digital number **CBA**, is created by attaching individual bits (**A**, **B** etc.):
  - to the 6V rail, to set them to logic 1,
  - to the 0V rail, to set them to logic 0.
- Switch on the 6V power supply.
- Connect inputs **A**, **B** and **C** to 0V, creating the binary number **000**. Note down the initial voltmeter reading in the first row of the table.
- Next, connect input **A** to 6V, and **B** and **C** to 0V, (binary number **001**), and record the new reading.
- Now, connect input **B** to 6V, and **A** and **C** to 0V, (binary number **010**). Again, note down the resulting reading.
- Continue in this way to input the other binary numbers, and complete the table with the corresponding output voltages.



Digital input	Analogue output
000	V
001	V
010	V
011	V
100	V
101	V
110	V
111	V

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Worksheet 11
The R-2R DAC

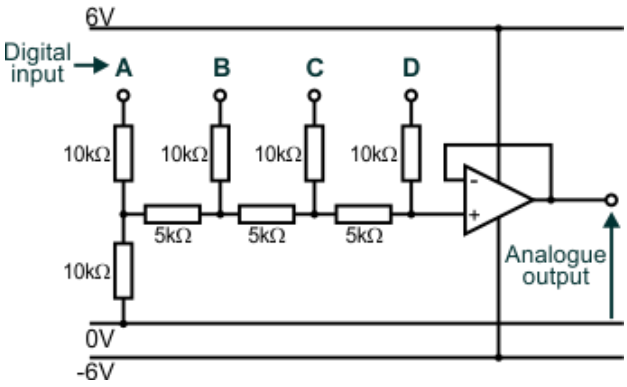
Sequential logic

So what?

- In a simple Digital-to-Analogue converter, the analogue output voltage should copy changes in the digital input number.
  - As the number gets bigger, the output voltage gets bigger.
  - When the number doubles, the output voltage should double, and so on.
- Look at your results table! Can you see this behaviour?
  Remember that all electronic components have manufacturing tolerances. Even though the resistors are high quality, they have a tolerance of 5%. The 10kΩ resistor may legitimately be anywhere between 9.5kΩ and 10.5kΩ.
- With this type of DAC, only two values of resistor are needed, one twice as big as the other.
  The accuracy of the conversion depends on having precise resistor values.
  The theory behind this circuit is quite complex, and is best tackled through Thevenin's theorem, which is beyond the scope of this course. Never mind the theory - it works!

Try this:

- Make a 4-bit R-2R ladder, and test it. (Your results table will need sixteen rows.)
- Replace the analogue voltmeter with a multimeter set onto the 20V range.
  The output voltage readings may rise by 30%! Why is this?
  Any device connected directly to the ladder acts like another resistor and affects the output voltage.
  An ideal voltmeter has infinite resistance, and draw no current from the R-2R ladder.
  The analogue voltmeter takes more current from the ladder circuit than the multimeter, reducing the voltage that appears at the output.
- Add a 'buffer' to the output of the R-2R ladder.
  In its simplest form, this produces an output voltage that copies the input. However, any current drawn from the output comes from the power supply, not from the ladder.
  An op-amp 'voltage follower' can be used for the job, as the circuit shows, but it will need a 'split' power supply, with an additional -6V supply.



For your records:

- Copy the circuit diagram for the 3-bit (unbuffered) DAC, given on the previous page.
- Copy your completed results table for the system.
- Add an explanation for why the output is bigger when a multimeter is used.
- Draw the circuit diagram for the 4-bit buffered DAC, using an op-amp voltage follower subsystem.

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Instructor Guide

Sequential logic

About this course

Introduction

The course is essentially a practical one. Locktronics equipment makes it simple and quick to construct and investigate electrical circuits. The end result can look exactly like the circuit diagram, thanks to the symbols printed on each component carrier.

Aim

The course introduces students to a range of common sequential logic systems. These form the basis for a deeper study of this topic.

Prior Knowledge

It is recommended that students have followed the 'Electricity Matters 1', 'Electricity Matters 2' and the 'Introduction to Combinational Logic' courses, or have equivalent knowledge, covering the basic electrical concepts of current, voltage and resistance, familiarity with logic gates both singly and in combinations and the construction and testing of circuits, using a range of measuring instruments.

Learning Objectives

On successful completion of this course the student will be able to:

- distinguish between combinational logic systems and sequential logic systems;
- distinguish between astable, monostable and bistable subsystems;
- compare the binary number system (with up to four bits) with its decimal equivalent;
- interpret timing diagrams that describe the behaviour of sequential systems;
- recognise voltage/time graphs for the output of monostable and astable systems;
- use the terms *amplitude*, *period, frequency, mark* and *space* to describe digital signals;
- relate period and frequency to the size of the timing components in astable and monostable subsystems ;
- use the formula for a 555 astable subsystem to calculate its frequency ;
- use the formula for a 555 monostable subsystem to calculate its delay ;
- draw the circuit diagram for a $\overline{S}\overline{R}$ bistable made from two NAND gates;
- complete a truth table for the $\overline{S}\overline{R}$ bistable;
- describe the behaviour of a rising-edge triggered D-type bistable;
- draw the timing diagram for a D-type, showing the relationship between clock, data and outputs;
- draw the circuit diagram for a latch made from a D-type bistable;
- draw the timing diagram for a D-type latch, showing the behaviour of the reset input;
- draw the circuit diagram and timing diagram for a one-bit counter made from a D-type bistable;
- draw the circuit diagram and timing diagram for a two-bit counter made from D-type bistables;
- explain why a one-bit counter is also known as a 'divide-by-two' subsystem;
- explain what is meant by 'switch bounce' and why it causes problems for counting systems;
- draw circuit diagrams for, and describe the principle of debouncing circuits that use a monostable or a bistable;
- explain how to reduce electrical noise in power rails using a decoupling capacitor;
- draw the circuit diagram and timing diagram for a three-bit counter made from D-type bistables;
- explain the meaning of 'modulo-n' counter;
- use an AND gate to reset a counter at a specified count;
- draw the circuit diagram and timing diagram for a three-bit shift register made from D-type bistables;
- distinguish between the following types of shift register - SISO, SIPO, PIPO, PISO;
- explain what is meant by 'DAC';
- draw the circuit diagram for a buffered four-bit R-2R DAC.

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Sequential logic

What the student will need:

To complete the sequential logic course, the student will need the following equipment:

- 2 LK8900 Locktronics Baseboards (0)
- 30 LK 5250 connecting links (7)
- 1 LK5202 1kΩ resistor carrier (0)
- 2 LK6230 5kΩ resistor carriers (2)
- 4 LK5203 10kΩ resistor carriers(0)
- 1 LK6231 50kΩ resistor carrier (0)
- 1 LK5218 100kΩ resistor carrier (1)
- 1 LK5224 47μF capacitor (1)
- 1 LK6202 100μF capacitor (1)
- 2 LK6207 push-to-make switch carriers (0)
- 1 LK6224 changeover switch (1)
- 1 LK6635 red LED carrier (0)
- 1 LK6636 green LED carrier (0)
- 1 LK6637 yellow LED carrier (1)
- 1 LK6860L AND gate carrier (0)
- 2 LK6863L NAND gate carriers (0)
- 1 LK7582L 555 timer carrier (1)
- 3 LK6500L D-type flip-flop carrier (3)
- 1 LK6503 systems block display decoder (1)
- 1 LK3982 voltmeter carrier (0)
- 1 6V DC power supply with carrier (0)
- 1 LK5603 4mm to 4mm lead red (0)
- 2 LK5604 4mm to 4mm lead black (0)
- 2 LK5607 4mm to 4mm lead yellow (0)
- 3 LK5609 4mm to 4mm lead blue(0)

The numbers in brackets are the parts needed if you already have the LK9071 Electricity, magnetism and materials kit AND the LK6904 Combinational logic add-on kit.

Using this course:

The experiments in this course should be integrated with teaching to introduce the theory behind it, and reinforced with written examples, assignments and calculations.

The worksheets should be printed / photocopied / laminated, preferably in colour, for the students' use. They should make their own notes, and carry out the tasks identified in the 'For your records' sections. They are unlikely to need their own permanent copy of the worksheets.

Each worksheet has:

- an introduction to the topic under investigation;
- step-by-step instructions for the investigation that follows;
- a section headed 'So What', to collate and summarise results, offer extension work and encourage development of ideas, through collaboration with partners and with the instructor.
- a section headed 'For your records', to be copied and completed in students' exercise books.

This format encourages self-study, with students working at a rate that suits their ability. The instructor should monitor that students' understanding keeps pace with their progress through the worksheets. One way to do so is to 'sign off' each worksheet, as a student completes it, and in doing so have a brief chat with the student to assess grasp of the ideas involved in the exercises it contains.

Time:

It should take students between 6 and 8 hours to complete the worksheets. It is expected that a similar

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Instructor Guide

Scheme of Work

Sequential logic

Worksheet	Notes for the Instructor	Timing
Intro	The aim here is firstly to distinguish between combinational and sequential systems and then to introduce the vocabulary of sequential systems. The essential ingredient in sequential systems is feedback. The current output state is determined not only by the current states of the inputs but also the previous states, as indicated by the output signal fed back to the inputs. For some students, the three types of 'flip-flop' cause confusion. It is worth driving home the differences at the beginning of the course to prevent any misunderstanding from hindering progress. As timing diagrams are introduced at this point, the instructor allow time for the students to become confident in interpreting them. Depending on the mathematical background of the students, the instructor may wish to introduce the binary number system by referring to the place values (2^0, 2^1, 2^2 etc.) involved.	**10 - 15 mins**
1	In this worksheet, students set up a 555 astable using the Locktronics carrier. This takes much of the effort out of the task. The investigation looks at the effect of different values of timing components on the frequency of the pulses produced. The text emphasises the need to time 'on's and 'off's, i.e. complete cycles. The instructor may need to reinforce this aspect. They time ten cycles in order to reduce errors in timing sort intervals. This could form part of a discussion on why measured values and calculated values are different. The average current taken by the 555 timer is tiny, but during the changes of state, logic 0 to 1 and 1 to 0, the current needed is enough to affect the power supply voltage, and add voltage spikes to it. These can cause problems for other devices in the system. To reduce these, the 555 carrier contains a decoupling capacitor, connected between the power rails. The electrical noise, the spikes, contain mainly high frequencies, which see the decoupling capacitor as an easy route to 0V. This reduces their magnitude, and the effect they have on the rest of the circuit. The worksheet includes descriptions of the square wave parameters *amplitude*, *period*, *frequency*, *mark*, *space* and *mark-to-space ratio*. The students convert their results using some of these parameters. They are then given the formula relating output frequency to the values of the timing components. Not the easiest formula to use, they are given some examples of its use before being asked to use it themselves. When they substitute the 100kΩ resistor for R_A, in the 'Try this' section, they should notice a radical change to the mark:space ratio.	**20 - 30 mins**

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Instructor Guide

Scheme of Work

Sequential logic

Worksheet	Notes for the Instructor	Timing
2	This worksheet carries out a similar examination of the 555 monostable sub-system. The output is triggered into its logic 1 state when the signal from the switch unit goes low for a moment, hence the orientation of the switch unit. The treatment looks at the delay caused by different sets of timing components. On the second page of the worksheet, three options are given for units when applying the formula to calculate the time period. To help the students with this, there is a reminder of what the multipliers 'kilo', 'mega' and 'micro' mean. The discussion comparing measured and calculated values is intended to bring out a range of factors like the accuracy of measuring relatively short time intervals and the tolerances of the components used. The final task is to use the formula given to calculate a resistor value suitable for a delay of eleven seconds.	**20 - 30 mins**
3	Many students will have difficulty in understanding what is happening here. The crux of NAND gate behaviour is: If any input is at logic 0, the output MUST be logic 1. If all we know is that one input is at logic 1, we do not know what the output will be. Suppose one of the outputs is logic 0. That signal is fed back to one of the inputs on the other gate and holds the output of that gate at logic 1. This, in turn, is connected to an input on the first gate. If the other input of that gate is at logic 1, (because of the pull-up resistors,) the output of that gate will be logic 0, and this is fed back and holds ….etc. The instructor may need to go through this argument a number of times before some students grasp its significance. The outcome is that the logic 0 signal from the switch forces the output to logic 1. When no switches are pressed, the output cannot change state. It is the logic 0 on one of the outputs that rules. In analysing the results table, the instructor should point out that it is different to the truth table used to describe combinational logic systems, because some input combinations, specifically the '1' '1' combination, crop up several times. The reason for this is the output is not determined by this set of inputs, but by the previous set. This is called the latching combination, as a result. The unfortunate combination is '0 '0'. This forces both NAND gate outputs to logic 1. There is nothing wrong with this electronically, and the NAND gates are quite happy. Unfortunately, it goes against our convention of wanting them to be in opposite states - the 'Q' and 'Q' idea. The 'So what' section shows how the limitations of this type of bistable are overcome in the D-type. The progression shown leads to what is called a level-triggered D-type, where the output can change state whenever the clock input is at logic 1. This lacks sufficient control of the output, and so the edge-triggered D-type is usually preferred, where the output is vulnerable to change for the very short period of time where the clock signal is rising from 0 to 1 (for rising-edge triggering.)	**30 - 40 mins**

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Sequential logic

Worksheet	Notes for the Instructor	Timing
4	The D-type bistable has a number of uses - for data transfer, as a latch, as a counter and as a register. We start by looking at the basic principle of its operation - that on the rising-edge of a clock pulse, i.e. for the brief instant when the logic level on the clock input changes from logic 0 to logic 1, the Q output copies the logic level it sees on the Data input. In the first part of the investigation, the student is taken through this sequence of signals. The instructor may wish to spend time at this point explaining the significance of the names 'pull-up' and 'pull-down' applied to resistors. One approach is to point out that an insignificantly small current flows in or out of the D-type input. With the switch open, no appreciable current flows through the resistor attached to it, and so, from Ohm's law, no voltage is dropped across it. In other words, both ends of the resistor are at the same voltage. In this case, we know that the bottom of the resistor is at 0V, and so the top (and hence the input to the D-type,) must also be at 0V. The input is 'pulled down' to 0V by the resistor. On the Locktronics D-type carrier, the Set and Reset inputs can be left disconnected. When using D-type chips, this practice should be avoided, as it can lead to undesirable results. If there are problems, the instructor should check that the power supplies to the bistable carrier are in place and correct. The second part, the latch, differs only in that the Data input is now permanently connected to logic 1 (6V). On the arrival of the rising-edge of a clock pulse, the Q output copies this and goes to logic 1 ('sets'). It then stays there. Further clock pulses have no effect, as the Data input is still at logic 1. The Reset (and Set) are termed asynchronous - they do not wait until a clock pulses arrives to take effect. As soon as the Rest input is taken to logic 1, it resets the Q output to logic 0. In all of this, the Q output sits in the opposite state to the Q output. $\bar{Q}$ This behaviour is then discussed in terms of timing diagrams.	**20 - 30 mins**
5	The development in this worksheet is that the $\bar{Q}$ output of the D-type is connected back to the Data input. This has a profound effect. The basic principle is unchanged - on the rising-edge of a clock pulse, the Q output copies the logic level it sees on the Data input. However, the Data input is now connected to $\bar{Q}$, which has the opposite state to Q. As a result, the Data input has the opposite state to the Q output. On each clock pulse, the output copies the Data input, and so changes state. The effect is seen by sending in a number of clock pulses using the push-switch. Any erratic behaviour is due to 'switch bounce', dealt with in the next worksheet. The reason for calling this a one-bit counter is that, in binary, the least significant bit of the number changes state in just this way, toggling between 0 and 1 as the number increases. The table comparing binary and decimal, in the introduction, shows this behaviour. These subsystems can be linked together to form multi-bit counters, as the second part of the worksheet shows. The second stage of the counter takes its clock pulse from the output of the first. It is significant whether the Q or the $\bar{Q}$ output is used to create this clock pulse. In the first case, the two-bit counter resulting counts down, whereas in the second, it counts up. The student investigates this effect in the '**challenge**' section. The behaviour of these variations is then displayed as timing diagrams.	**40 - 50 mins**

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Instructor Guide

Scheme of Work

Sequential logic

Worksheet	Notes for the Instructor	Timing
6	The student will probably have seen some erratic behaviour in the previous worksheet. Sometimes, the sequence of outputs seems to jump one or more steps. The cause is switch bounce. By necessity, switches contain springy metal contacts. Inevitably, when forced together, they try to bounce apart again. Normally, this is not a problem. We don't notice any adverse effect when we switch on a room light, for example. However, if an electronic system is set up to count electrical pulses, there will be problems. What we want is each press of the switch to produce one pulse. One approach is to mask any additional 'bounce' pulses, by keeping the signal at logic 1 until the bouncing dies away. That is the approach explored here. A monostable subsystem provides clock pulses for the counter. It is triggered by a pulse from the switch. However, the 'bounce' pulses do not appear at the output of the monostable. The output just sits at logic 1. There is an optimum time delay for a given counting system. If the delay is too long, then some valid pulses may be missed. If the delay is too short, then some 'bounce' pulses may cause false triggering, and clock pulses. It is possible that some electrical noise may appear on the power rails, and cause false triggering of the counter. The student is advised to add a further large value decoupling capacitor between the power rails. The instructor should check that the correct polarity is observed if this is done.	**25 - 40 mins**
7	This worksheet looks at the 'Rolls-Royce' of debouncing systems - the use of a bistable. In practice, it may not be suitable, as many sensors operate like a single-pole-single-throw switch, whereas this requires a single-pole-double-throw switch. The introduction revisits the use of a monostable, representing its behaviour as voltage/time graphs. The instructor may choose to spend significant time going over the diagrams of the NAND gate bistable, given on the second page of the worksheet. Otherwise it is likely to re-ignite the problems highlighted earlier for this subsystem. The important point is that the switch will still bounce, but that when it happens, the bistable goes into its '1' '1' state, and latches. The bounces send no further pulses to the counter. The worksheet suggests that the student use an oscilloscope to see the switch bounce. This can be a time-consuming activity. The instructor may decide to do this as a class demonstration.	**30 - 40 mins**
7A	To streamline progress through the next three worksheets, it is suggested that the student assemble a debounced switch, using a NAND gate bistable, on a separate board. This can be used in conjunction with a second board, on which the additional subsystem is created.	**15 - 25 mins**

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Scheme of Work

Sequential logic

Worksheet	Notes for the Instructor	Timing
8	Now, the student sees a fully-functioning debounced switch (on its own base-board,) generating clock pulses for a 3-bit counter. The counting sequence it produces should be error-free. To check the results, or restart the sequence, simply send in enough clock pulses to turn off all three LEDs. Alternatively, attach a lead to connect each of the Reset inputs to logic 1. (Don't forget to remove them when the sequence is supposed to start!) The analysis in the 'So what' section compares the sequence obtained to the binary count shown in the introduction, to demonstrate that this system counts up in binary. Finally, the student modifies the arrangement so that successive clock pulses are taken from the Q output, rather than the $\overline{Q}$. The effect should be that the counter counts down. Again, comparison with the table from the introduction should show this. Chips are mass-produced, and therefore vary slightly in per-formance. It is possible that the signal from the Q output may not be strong enough to 'clock' the next stage, because of the loading effect of the LED. If this is the case, temporarily remove the LED carrier from the output.	**30 - 40 mins**
9	The imposing title 'modulo-n' simply means that the counter can be made to reset at any count, i.e. on the n^{th} clock pulse. The only pitfall is forgetting that zero is included in this. A modulo-10 counter resets on the tenth clock pulse (almost immediately,) so that the biggest, stable, number it can show is '9'. To achieve this control, all the Reset inputs are connected to the output of an appropriate logic system, which generates a logic 1 output on the desired clock pulse, to reset the counter. (Some D-type counters reset on receiving logic 0 signals on their Reset inputs. To show this, the input is marked as '$\overline{R}$', or has an 'inversion bubble' (circle) on it.) In the system created here, the logic system is a single 2-input AND gate, with its inputs connected to Q_C and Q_A. As a result, it resets when both of these are first high, i.e. on the fifth clock pulse. It is a modulo-5 counter - the highest stable count possible is '100_2' ('4').	**20 - 30 mins**
10	While students intuitively know what a counter does, the same is not true for shift registers. Taking each word separately, they are registers, which in electronics and computing means a subsystem capable of storing a binary number, and they shift that number in and out either in serial fashion, (one bit at a time,) or in parallel fashion, (all bits at once). Students confuse counter and shift-register circuits, when made from D-type bistables. It is well worth the instructor driving home each of the differences set out in the worksheet. In expressing the results of the investigation, students might find the timing diagrams a challenge. To reinforce them and test the student's understanding, the instructor could provide alternative versions, where the number of clock pulses, or the data signal is different. Students, individually or in groups, could be set the task of researching the different types of shift register on the internet, or using reference books. The outcome could be to present a talk on one type to the rest of the group, to create a display or a write a description.	**30 - 40 mins**

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Scheme of Work

Sequential logic

Worksheet	Notes for the Instructor	Timing
11	This worksheet introduces the topic of digital-to-analogue conversion, using a basic system - the R-2R ladder. The instructor may wish to introduce the topic by wider reference to the use of DACs and ADCs in microprocessor systems. The circuit is simple to set up and use, but the circuit analysis is complex, and not attempted in this course. Should the instructor wish to incorporate this, it is suggested that it starts with a simpler system - a 2-bit DAC. The moving-coil voltmeter carrier is sufficient to illustrate the trend - that increasing the binary number increases the analogue output voltage. Like most moving-coil meters, it does draw a significant current to operate. This affects the readings produced in the exercise, but not the overall effect. The instructor may wish to replace it with a digital multimeter, which draws a much smaller current. However, using both, separately, can lead to a useful discussion about circuit loading. It points to the need for a buffer if the ladder is to be used as part of a larger system. The instructor may need to amplify the content to explain the role of a buffer subsystem, and in particular explain that the current drawn by the subsequent components comes directly from the power supply to the buffer, and not from the ladder itself. The students are asked to add a voltage follower, using an op-amp, as a buffer. The instructor may wish to demonstrate this as a separate system, and could introduce it as a non-inverting voltage amplifier with a zero ohms feedback resistor and infinite input resistor, giving it a voltage gain of unity.	**30 - 40 mins**

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Apparatus for this course

Most of the apparatus for this course is available as Matrix product LK6905 ‘Sequential Logic add-on kit’. Please note however…

- It is assumed that a power supply capable of supplying up to 12V DC at 500mA is available.
- It is assumed that a selection of 4mm to 4mm (“banana”) leads are available.
- It is assumed that apparatus from the following Locktronics kits will be available…
  LK9071—Electricity Matters
  LK6904—Combination Logic add-on kit.

Version Control

Version	Released	Notes
LK9945-80-01	2015 June 02	First public release
LK9945-80-02	2017 July 26	Updates to use LK7582 555 timer carrier

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